INTERNATIONAL DATA SCIENCES INC.

OPERATION MANUAL
FOR
IDS BERT (MODELS 76B AND 77)
INTERFACE MODULES

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# FOR
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# OPERATION MANUAL FOR IDS BERT INTERFACE MODULES

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# BERT INTERFACE MODULE SUMMARY

## RS-232-C

| | |
|---|---|
| Interface Specs | RS-232-C, CCITT V.24 |
| Monitor LEDs | TD, RD, RTS, CTS, DTR, DSR, TCE, DCD, TC, RC |
| Interf.Connector | 25 pin, male, D-type. |
| Speed | Up to 64 Kbps |

## V.35

| | |
|---|---|
| Interface Spec | CCITT V.35 |
| Signal Control | LT (Local Test) |
| Monitor LEDs | SD, RD, RTS, CTS, DTR, DSR, SCTE, RLSD, LT, SCT, SCR |
| Interf. Connector | 34 pin, male, Winchester-type. |
| Speed | Up to 2.048 Mbps. Up to 6.312 MHz with SCTE clock. |

## RS-449-B (balanced)

| | |
|---|---|
| Interface Specs | RS-449, RS-422, RS-423 |
| Signal Control | LL (Local Loopback), RL (Remote Loopback) |
| Monitor LEDs | SD, RD, RS, CS, TR, DM, TT, RR, LL, ST, RL, RT |
| Interf. Connector | 37 pin, male, D-type. |
| Speed | Up to 10 Mbps |

## EIA-530

| | |
|---|---|
| Spec | EIA-530 |
| Signal Control | LL (Local Loopback), RL (Remote Loopback), |
| Monitor LEDs | TD, RD, RTS, CTS, DTR, DCR, TSET (DTE),RLSD, LL, TSET (DCE), RL, RSET |
| Connector | 25-pin, male, D-type |
| Speed | to 10 Mbps |

## MIL188-114

| | |
|---|---|
| Interf. Spec | MIL 188-114 |
| Monitor LEDs | SD, RD, RS, CS, TR, DM, RR, ST, RT, TT |
| Interf. Connector | 37 Pin, male, D-type. |
| Speed | Up to 10 Mbps |

## X.21

| | |
|---|---|
| Spec | CCITT X.21 |
| Transmitter | Differential output |
| Receiver | Differential input |
| Monitor LEDs | T, R, C, I, B, S |
| Connector | 15-pin, male, D-type. |
| Speed | To 10 Mbps |

## G.703 (2 Modules)

| | |
|---|---|
| Interface Spec | G.703 |
| **64 Kbps Co-directional** | Internal or recovered clock, 120 ohm balanced, |
| Interf. Connector | 25 pin, male, D-type. |
| **8.448 Mbps** HDB3 | Internal Tx clock, recovered Rx clock. 75 ohm co-axial connector |

## DS1/T1

| | |
|---|---|
| Interface Spec | AT& T Pub. 62411, CB144, Issue 1 |
| Framing Format | Unframed, D4 ($F_t$), D4 ($F_t$, $F_s$), ESF |
| Line Code | AMI or B8ZS |
| Tx Timing | Internal 1.544 MHz, Loop (recovered receive clock) |
| Rx Impedance | Terminate (100 ohms), Bridge ( > 1K ohms) |
| Alarms | Loss of Carrier, Loss of Local and Remote Frame Sync (Red and Yellow Alarms) |
| Monitor LEDs | SD and RD |
| Interf. Connector | 15 pin, female, D-type with 310, and Bantam adapters available. |
| Speed | 1.544 Mbps |

## T1/FRACTIONAL T1

| | |
|---|---|
| Spec | AT&T Pub. 62411, CB144, Issue 1 |
| Framing | Unframed, D4 (Ft), D4 ($F_t$, $F_s$), ESF |
| Line Code | AMI, B8ZS |
| Tx Timing | Internal 1.544 MHz, Loop (recovered receive clock) |
| Rx Impedance | Terminate (100 ohms), Bridge ( > 1K ohms). |
| Test Config. | Full T1, Fractional T1, Active Channel Detect. |
| Channel Rate | 56 kHz |
| Line Build-Out | 0 dB, -7.5 dB, -15 dB. |
| Rx Level Meter | Ten red LEDs in 3 dB increments |
| Alarm LEDS | RED (red LED), YELLOW (yellow LED), BLUE (red LED), LOSS OF CARRIER (yellow LED) |
| Active Channel LEDS | 24 green LEDs indicate which of 24 channels contain data or idle characters. |
| DS0 Channel Select | 24 switches select the channel contents (Data or Idle) |
| Audible Alarm | Sounds on alarm conditions, memory failure, illegal settings. Disable with ON/OFF switch. |
| Speed | 1.544 Mbps |

## E1/FRACTIONAL E1

| | |
|---|---|
| Interface Specs | G.703, G.704, G.732 |
| Framing Format | Unframed, CCS, CAS |
| Line Code | AMI or HDB3 |
| Rx Impedance | 75 ohms, 120 ohms, Bridge ( > 1 K ohms) |
| Test Config | Full E1, Fractional E1, Active TS Detect |
| Tx Timing | Internal (2.048 MHz crystal) Recovered (from receive data) External (BNC TTL input) |
| Time Slot LEDs | Thirty-two (32) green LEDs indicate which of the time slots contain data or idle characters |
| TS Select Switches | Thirty-two (32) dip switches select time slot contents (Data or Idle) |
| Fault & Alarm LEDs | NO FA<br>NO MFA<br>LOSS OF SIGNAL<br>AIS (64 K)<br>AIS (2 M)<br>REMOTE ALARM<br>REMOTE MF ALARM |
| Audible Alarm | Activated for alarm and fault conditions, memory failure, illegal switch settings. Audible ON/OFF switch selectable |
| Speed | 2.048 Mbps |

## T1/FT1 DATA/VF DROP AND INSERT

| | |
|---|---|
| Spec | AT&T Pub. 62411, CB144, Issue 1. |
| T1 Framing | D4, ESF, SLC-96, Unframed |
| Tx Timing | Loop or Internal |
| Line Code | AMI or B8ZS |
| DS0 Rate | 56K or 64K |
| T1 Receiver | Bridge, Terminate, or Monito ALBO, Bantam Jack |
| T1 Transmitter | Compatible with DSX-1 or Long Haul, Bantam Jack. |
| Line Build Out | 0 dB, -7.5 dB, -15 dB |
| Fractional T1 | Contiguous or non-contiguous channels in any combination, can operate in Drop & Insert mode. |
| Active Channel Detect | Detects which channels are not idle, 24 LEDs display active channel. |
| VF | Test any channel, Mu-Law CODEC, can operate in Drop & Insert mode. |
| VF Insert Source | Digital milliwatt, Idle, or external VF-in bantam jack. |
| VF Output | Internal Speaker and external VF-out bantam jack, PCM digital data displayed in 8 LEDs. |
| Tx Signalling | D4 and SLC-96 A and B bits set to 0, 1, alternate 0/1, or disabled. ESF A, B, C & D bits set to 0, 1 or disabled |
| Rx Signalling Alarm and Error LEDs | Displayed on 4 LEDs Red, Yellow, Blue, BPV, Frame/CRC Error, Excess Zeros, Loss of Signal, Setup Error |

## DDS LOCAL LOOP

| | |
|---|---|
| Setup | Pushbutton, Automatic |
| Power | +5Vdc, 320 mA Max.<br>+12Vdc, 93 mA Max.<br>-12 Vdc, 43 mA Max. |
| DDS Output | 135 ohm, 0.88V |
| DDS Input | Switchable 135 ohm or > 1K ohm impedance<br>Automatic equalization and Extended range indication |
| Internal Clock | Accuracy: 50 ppm |
| Level Meter | |
| Range | .0V to 3.0V peak |
| Resolution | 0.01V, 1 dB |
| Accuracy | +/- 5% |
| Sealing Current | 3.9 to 4.1 mA |

## Introduction

IDS Interface Modules provide the IDS BERT testers with complete in-house and field-testing capability. All interface modules are of sturdy construction with durable polypropylene housing. The front-panel label is easy-to-read Lexan. Modules are attached to the base unit, easily and firmly, with a thumbscrew.

**Please note: (For users of the Model 76B only) Do not insert any module into the Model 76B while the power is on.**

This manual is divided into sections that describe each individual module. If you have any questions, please do not hesitate to call our technical support staff at 1-800-IDS-DATA (1-800-437-3282). We will be pleased to assist you.

## Introduction

The RS-232 interface module provides the physical and electrical interface between the base unit and a DCE.

The module consists of a 25-pin, male, "D" connector with threaded female standoffs for mating connector attachment. The interface conforms to EIA-RS-232-C and CCITT V.24 and V.28 standards.

This interface will operate at data rates up to 20 kbps over 50 feet of standard RS-232 cable or up to 250 feet of low capacitance cable. Data rates of up to 64 kbps will operate over shorter cable lengths.

## Interface Connectors

The RS-232-C interface module has two connectors. A 37-pin male "D" connector, located on the back panel provides the connection to the base unit.

A 25-pin, male "D" connector, located at the top of the front panel provides the connection to the DCE. The pin assignment for this connector follows. A thumb screw, located in the center of the module provides a means for firmly attaching the module to the base unit.

RS-232-C INTERFACE CONNECTOR PIN ASSIGNMENTS

| Pin # | Name | Direction | | Circuit | | Description |
|---|---|---|---|---|---|---|
| | | To DTE | To DCE | EIA | CCITT | |
| 1 | FG | | | AA | 101 | Frame Ground — This lead is an electrical equipment frame and power ground. |
| 2 | TD | | ⇒ | BA | 103 | Transmitted Data — This lead carries the serial digital data transmitted from the DTE to the DCE. |
| 3 | RD | ⇐ | | BB | 104 | Received Data — This lead carries the serial digital data received at the DTE. |
| 4 | RTS | | ⇒ | CA | 105 | Request to Send — An ON condition on this lead is used to enable the local DCE for data transmission. |
| 5 | CTS | ⇐ | | CB | 106 | Clear to Send — An ON condition on this lead indicates whether or not the DCE is ready to transmit data. |
| 6 | DSR | ⇐ | | CC | 107 | Data Set Ready — An ON condition on this lead indicates that the local DCE is ready to process data and is not in a test, talk, or dial mode. |
| 7 | SG | | | AB | 102 | Signal Ground — This lead establishes the common ground reference potential for all circuits except frame ground on Pin 1. |
| 8 | DCD | ⇐ | | CF | 109 | Data Carrier Detect (Received Line Signal Detector) - This lead indicates that the data from the remote location is being received and meets suitable criteria established by the DCE manufacturer. |
| 9 | — | | | | | Not Used |
| 10 | — | | | | | Not Used |
| 11 | — | | | | | Not Used |
| 12 | — | | | | | Not Used |
| 13 | — | | | | | Not Used |
| 14 | — | | | | | Not Used |
| 15 | TC | ⇐ | | DB | 114 | Transmitter Clock — This lead is used to provide the DTE with signal element timing information. |
| 16 | — | | | | | Not Used |
| 17 | RC | ⇐ | | DD | 115 | Receiver Clock — This lead is used to provide the DTE with received signal element timing information. |
| 18 | — | | | | | Not Used |
| 19 | — | | | | | Not Used |

(Continued)

(Continued)

| | | | | | | |
|---|---|---|---|---|---|---|
| 20 | DTR | | ® | CD | 108.2 | Data Terminal Ready — An ON condition on this lead indicates that the DTE is ready to be connected to the communication channel. |
| 21 | — | | | | | Not Used |
| 22 | RI | ← | | CE | 125 | Ring Indicator — An ON condition on this lead indicates that a ringing signal is being received on the communication channel. |
| 23 | — | | | | | Not Used |
| 24 | TCE | | ® | DA | 113 | External Transmitter Clock — This lead is used to provide the transmitting signal converter with signal element timing information. |
| 25 | — | | | | | Not Used |

**Driver Outputs (unloaded)**

| | |
|---|---|
| Binary One | - 8V to - 15V |
| Binary Zero | + 8V to +15V |
| Output Impedance | 300 ohms minimum |
| Control Signals On, Space | + 8V to + 15V |
| Control Signals Off, Mark | - 8V to - 15V |
| Protection | All outputs are protected against damage caused by accidental shorting up to 25V. |

**Receiver Inputs**

| | |
|---|---|
| Binary One | - 3V to - 25V |
| Binary Zero | + 3V to +25V |
| Input Impedance | 3000 ohms to 7000 ohms |
| Protection | +/-25 volts without damage to receiver circuits. |

## SPECIFICATIONS

| | |
|---|---|
| Dimensions | 5.25" L x 4.2" W x 1.17" H (13.33 cm x 10.67 cm x 2.98 cm) |
| Weight | 12 oz. (340 gm) |
| Temperature | Operating: 0°C to 50°C (32°F to 122°F) |
| | Storage: -10°C to 55°C (14°F to 131°F) |
| Relative Humidity | 90% maximum, non-condensing |

### Introduction

IDS Interface Modules provide the IDS BERT testers with complete in-house and field-testing capability. The front-panel label is easy-to-read Lexan. Modules are attached to the base unit, easily and firmly, with a thumbscrew.

### V.35 Interface Module

The V.35 interface module provides the physical and electrical interface between the Model 77 or 76B Bit Error Rate Test Set (base unit) and a V.35 type DCE.

The V.35 interface module has two connectors. A 37-pin male "D" connector located on the back panel provides the connection to the base unit. A 34-pin, male, Winchester type connector provides the physical interface and the electrical interface conforms to the CCITT V.35 specification.

Eleven interface signals (SD, RD, RTS, CTS, DTR, DSR, SCTE, RLSD, LT, SCT and SCR) are monitored by the LEDs on the base unit. Each mnemonic label is located on the interface module LEXAN above its appropriate LED. A two-position slide switch, labeled OFF and ON allows the user to control the Local Test (LT) interface signal to the DCE for testing purposes when applicable.

### Speed

The interface will operate up to 2.048 MHz with an internal base unit rate or a clock sourced by SCT. If the realigned clock at SCTE is used, the interface will operate up to 6.312 MHz.

### Interface Connector Pin Assignments

V.35 INTERFACE CONNECTOR - PIN ASSIGNMENTS

| MIL PIN | COMM PIN | MNEMONIC NAME | DIRECTION TO DTE | DIRECTION TO DCE | FUNCTION |
|---|---|---|---|---|---|
| A | A | FG | | | Frame (protective) Ground |
| B | B | SG | | | Signal (Reference) Ground |
| C | C | RTS | | ⇒ | Request To Send |
| D | D | CTS | ⇐ | | Clear To Send |
| E | E | DSR | ⇐ | | Data Set Ready |
| F | F | RLSD | ⇐ | | Received Line Signal Detector |
| H | H | DTR | | ⇒ | Data Terminal Ready |
| J | J | RI | ⇐ | | Ring Indicator |
| K | K | LT | | ⇒ | Local Test |
| L | L | – | | | Unused |
| M | M | – | | | Unused |
| N | N | – | | | Unused |
| P | P | SD(A) | | ⇒ | Send Data (Signal A) |
| R | R | RD(A) | ⇐ | | Received Data (Signal A) |
| S | S | SD(B) | | ⇒ | Send Data (Signal B) |
| T | T | RD(B) | ⇐ | | Received Data (Signal B) |
| U | U | SCTE(A) | | ⇒ | Serial Clk. Xmit Ext. (Sig. A) |
| V | V | SCR(A) | ⇐ | | Serial Clk. Receive (Sig. A) |
| W | W | SCTE(B) | | ⇒ | Serial Clk. Xmit Ext. (Sig. B) |
| X | X | SCR(B) | ⇐ | | Serial Clk. Receive (Sig. B) |
| Y | Y | SCT(A) | ⇐ | | Serial Clk. Xmit (Sig. A) |
| Z | Z | – | | | Unused |
| AA | a | SCT(B) | ⇐ | | Serial Clk. Xmit (Sig. B) |
| b, c, d, f, g, h, i, j, k, m n (Unused) BB, CC, DD, EE, FF, HH, JJ, KK, LL, MM, NN (Unused) | | | | | |

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### Balanced Driver Outputs (V.35)

| | |
|---|---|
| Binary One, Mark, Off | Output A negative with respect to output B |
| Binary Zero, Space, On | Output A positive with respect to output B |
| Levels - terminated | 0.55V peak (1.1V +/- 20% peak-to-peak |
| Rise time (10% - 90%) | Less than 1% of the clock period or 40 ns, whichever is greater |
| Fall time (10% - 90%) | Less than 1% of the clock period or 40 ns, whichever is greater |
| Output Impedance | 100 ohms +/- 10% |
| Resistance to GND | 150 ohms +/- 10% (A & B leads shorted together |
| DS Offset | 0.6V max. (arithmetic mean of A to ground and B to ground) |

### Single-ended Driver Outputs (RS-232-C)

| | |
|---|---|
| Binary One, Mark, Off | -8V to -12V (terminated) |
| Binary Zero, Space, On | +8V to +12V (terminated) |
| Output Impedance | 300 ohms, minimum |

### Balanced Receiver Inputs (V.35)

| | |
|---|---|
| Binary One, Mark, Off | A negative with respect to output B |
| Binary Zero, Space, On | A positive with respect to output B |
| Levels | 0.55V peak (1.1V +/- 20% peak-to-peak |
| Input Impedance | 100 ohms +/- 10% |
| Resistance to GNC | 150 ohms +/- 10% (A & B leads shorted together) |

### Single-ended Receiver Inputs (RS-232-C)

| | |
|---|---|
| Binary One, Mark, Off | -3V to -25V |
| Binary Zero, Space, On | +3V to +25V |
| Input Impedance | 3k ohms to 7k ohms |

### Specifications

| | |
|---|---|
| Dimensions | 5.25"H x 4.20"W x 0.87"D (13.34 cm x 10.67 cm x 2.21 cm) |
| Weight | 7.5 oz. (213 gm) |
| Temperature | Operating: 0°C to 50°C (32°F to 122°F) |
| Relative Humidity | 90% maximum, non-condensing |

### Introduction

The RS-449-B interface module provides the data, control, and clocking necessary to perform tests in the RS-449 environment. The module contains the necessary drivers and receivers to allow the base unit to communicate with the outside world. A three-position slide switch allows the user to exercise either the Local Loopback (LL) or the Remote Loopback (RL), if required. The drivers conform to RS-422 (Balanced) for data and clocking signals and to RS-423 (Single-Ended) for control signals. Twelve (12) interface signals are monitored by the base unit LEDs. Each LED's function is defined by the mnemonic name located on the front panel Lexan adjacent to the associated LED.

The interface to the user's DCE is through a 37-pin, female, "D" type connector, located on the front panel of the RS-449-B interface module. A 37-pin, male, "D" type connector, located on the rear panel, provides the connection to the base unit. A thumbscrew, located in the center of the module, provides a means to firmly attach the module to the base unit.

### Base Unit Connector

The RS-449-B interface module has a 37-pin "D" type connector (male) on its back panel. This connector mates to the connector on the base unit when the interface module is plugged in.

### Front Panel Description

### Interface Connector

Interface to the DCE is accomplished by a 37-pin male "D" type connector. The signals used on this connector are SD, RD, ST, RT, TT, RS, CS, DM, RR, TR, TM, LL, and RL. The pin designations for this connector follow.

RS-449-B INTERFACE CONNECTOR PIN ASSIGNMENTS

| Pin # | Mnemonic Name | Direction To DTE | Direction To DCE | Function |
|---|---|---|---|---|
| 1 | | | | Shield |
| 2 | – | | | Not Used |
| 3 | – | | | Not Used |
| 4 | SD | | ⇒ | Send Data A |
| 5 | ST | ⇐ | | Send Timing A |
| 6 | RD | ⇐ | | Receive Ready A |
| 7 | RS | | ⇒ | Request to Send A |
| 8 | RT | ⇐ | | Receive Timing A |
| 9 | CS | | | Clear to Send A |
| 10 | LL | | ⇒ | Local Loopback |
| 11 | DM | ⇐ | | Data Mode A |
| 12 | TR | | ⇒ | Terminal Ready A |
| 13 | RR | | | Receiver Ready A |
| 14 | RL | | ⇒ | Remote Loopback |
| 15 | – | | | Not Used |
| 16 | – | | | Not Used |
| 17 | TT | | | Terminal Timing A |
| 18 | TM | ⇐ | | Test Mode |
| 19 | SG | | | Signal Ground |
| 20 | RC | ⇐ | | Receive Common |
| 21 | – | | | Not Used |
| 22 | SD | | | Send Data B |
| 23 | ST | | | Send Timing B |
| 24 | RD | ⇐ | | Receive Data B |
| 25 | RS | | ⇒ | Request to Send B |
| 26 | RT | ⇐ | | Receive Timing B |
| 27 | CS | ⇐ | | Clear to Send B |
| 28 | – | | | Not Used |
| 29 | DM | ⇐ | | Data Mode B |
| 30 | TR | | ⇒ | Terminal Ready B |
| 31 | RR | ⇐ | | Receiver Ready B |
| 32 | – | | | Not Used |
| 33 | SQ | ⇐ | | Signal Quality |
| 34 | – | | | Not Used |
| 35 | TT | | ⇒ | Terminal Timing B |
| 36 | – | | | Not Used |
| 37 | SC | | ⇒ | Send Common |

### Remote Loop/Local Loop Switch

A three-position slide switch allows the user to exercise either the Local Loopback (LL) or the Remote Loopback (RL), if interfacing to a modem which is capable of performing these functions.

### Monitored Signals

Twelve (12) interface signals are monitored by the base unit. The signal mnemonics are located on each side of the interface module front panel Lexan to identify the appropriate LED on the base unit. The interface signals monitored by the base unit are SD, RD, RS, CS, TR, DM, TT, RR, ST, RT, LL, and RL.

### Driver Outputs

| | |
|---|---|
| Binary One (Mark), Off | A negative with respect to B |
| Binary Zero (Space), On | A positive with respect to B |
| Driver Impedance (Zout) | 100 ohms +/- 1% balanced<br>50 ohms +/- 1% single ended |

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| | |
|---|---|
| Rise and Fall Time | Greater than 20 nanoseconds when measured between 10% and 90% of rise or fall |
| Driver DC Offset | 0V +/- 0.5V balanced<br>0V +/- 0.25V single ended |
| Driver Protection | Outputs short circuit protected to ground or to each other (150 mA maximum) |

**Receiver Inputs**

| | |
|---|---|
| Binary One (Mark), Off | A negative with respect to B |
| Binary Zero (Space), On | A positive with respect to B |
| Receiver Sensitivity | +/- 200 mV maximum balanced<br>+/- 400 mV maximum single ended |
| Receiver Impedance (Zin) | 2000 ohms minimum balanced<br>4000 ohms minimum single ended |
| Receiver DC Offset | +/- 7V maximum for proper operation |
| Receiver Protection | +/- 15V maximum without damage to receiver circuits |

## SPECIFICATIONS

| | |
|---|---|
| Dimensions | 5.25" x 4.20" x 0.87"<br>(13.34 cm x 10.67 cm x 2.21 cm) |
| Weight | 7.5 oz (213 gm) |
| Temperature | Operating: 0°C to 50°C<br>(32°F to 122°F) |
| Relative Humidity | 90% maximum, non-condensing |

### Introduction

The EIA-530 Interface Module provides the data, control, and clocking signals necessary to perform tests in the EIA-530 environment. It contains the necessary drivers and receivers to allow the base unit to communicate with the outside world.

The interface is configured as a DTE. A three-position slide switch allows the user to exercise either the Local Loopback (LL) or the Remote Loopback (RL), if required. The drivers and receivers conform to EIA-423 (Single-ended) for the RL, LL and TM signals and to EIA-422 (Balanced) for all other signals.

### Base Unit Connector

The EIA-530 Interface Module has a 37-pin D-type connector (male) on its back panel. This connector mates to the connector on the base unit when the interface module is plugged in.

### Front Panel Description

### Interface Connector

Interface to the DTE is accomplished by a 25-pin male D-type connector. The signals used on this connector are TD, RD, RTS, CTS, DCR, RLSD, TSET (DCE Source), RSET, LL, DTR, RL, TSET (DTE Source), TM. See the following table for pin assignments.

EIA-530 INTERFACE CONNECTOR PIN ASSIGNMENTS

| Pin # | Mnemonic Name | Direction To DTE | Direction To DCE | Function |
|---|---|---|---|---|
| 1 | Shield | | | Shield |
| 2 | TD (A) | | ➡ | Transmitted Data (A) |
| 3 | RD (A) | ⬅ | | Received Data (A) |
| 4 | RTS (A) | | ➡ | Request to Send (A) |
| 5 | CTS (A) | ⬅ | | Clear to Send (A) |
| 6 | DCR (A) | ⬅ | | DCE Ready (A) |
| 7 | SG | | | Signal Ground |
| 8 | RLSD (A) | ⬅ | | Received Line Signal Detector (A) |
| 9 | RSET (B) | ⬅ | | Receiver Signal Element Timing (B) |
| 10 | RLSD (B) | ⬅ | | Received Line Signal Detector (B) |
| 11 | TSET (B) | | ➡ | Transmit Signal Element Timing, DTE Source (B) |
| 12 | TSET (B) | ⬅ | | Transmit Signal Element Timing, DCE Source (B) |
| 13 | CTS (B) | ⬅ | | Clear to Send (B) |
| 14 | TD (B) | | ➡ | Transmitted Data (B) |
| 15 | TSET (A) | ⬅ | | Transmit Signal Element Timing, DCE Source (A) |
| 16 | RD (B) | ⬅ | | Received Data (B) |
| 17 | RSET (A) | ⬅ | | Receiver Signal Element Timing (A) |
| 18 | LL | | ➡ | Local Loopback |
| 19 | RTS (B) | | ➡ | Request to Send (B) |
| 20 | DTR (A) | | ➡ | DTE Ready (A) |
| 21 | RL | | ➡ | Remote Loopback |
| 22 | DCR (B) | ⬅ | | DCE Ready (B) |
| 23 | DTR (B) | | ➡ | DTE Ready (B) |
| 24 | TSET (A) | | ➡ | Transmit Signal Element Timing, DTE Source (A) |
| 25 | TM | ⬅ | | Test Mode |

### Remote Loop/Local Loop Switch

A three-position slide switch allows the user to exercise either the Local Loopback (LL) or the Remote Loopback (RL), if required.

### EIA-530 Interface Connector Pin Assignments

The EIA-530 Interface connector pin assignments are shown in in the preceding table.

The following lines are driven: TD, RTS, DTR, TSET, (DTE Source), LL and RL.

The following lines are received: RD, CTS, DCR, RLSD, TSET (DCE Source), RSET and TM.

LL and RL are under the control of the Remote Loop/Local Loop switch on the base unit.

### Driver Outputs

| | |
|---|---|
| Binary One (Mark), Off | A negative with respect to B |
| Binary Zero (Space), On | A positive with respect to B |
| Driver Impedance (Z out) | 100 ohms +/- 1% balanced<br>50 ohms +/- 1% single ended |
| Rise and Fall Time | Greater than 20 nanoseconds when measured between 10% and 90% of rise or fall |
| Driver DC Offset | 0V +/- 0.5V balanced<br>0V +/- 0.25V single ended |
| Driver Protection | Outputs short circuit protected to ground or to each other (150 mA maximum. |

**Receiver Inputs**

| | |
|---|---|
| Binary One (Mark), Off | A negative with respect to B |
| Binary Zero (Space), On | A positive with respect to B |
| Receiver Sensitivity | +/- 200 mV maximum balanced<br>+/- 400 mV maximum single ended |
| Receiver Impedance (Z in) | 2000 ohms minimum balanced<br>4000 ohms minimum single ended |
| Receiver DC Offset | +/- 7V maximum for proper operation |
| Receiver Protection | +/- 15V maximum without damage to receiver circuits |

## SPECIFICATIONS

| | |
|---|---|
| Dimensions | 5.25" x 4.20" x 0.87"<br>(13.34 cm x 10.67 cm x 2.21 cm) |
| Weight | 7.5 oz. (213 gm) |
| Temperature | Operating: 0°C to 50°C<br>(32°F to 122°F)<br><br>Storage: -10°C to 55°C<br>(14°F to 131°F) |
| Relative Humidity | 90% maximum, non-condensing |

### Introduction

The MIL 188-114 interface module provides the base unit with data, control, and clocking signals necessary to perform tests in the MIL 188-114 environment at data rates up to 300 kbps.

### Base Unit Connector

The MIL 188-114 has a 37-pin "D" type connector (male) on its back panel. This connector mates to the connector on the base unit when the interface module is plugged in.

### Interface Connector

Interface to the DCE is accomplished by a 37-pin male "D" type connector. The signals used on this connector are SD, RD, RS, CS, TR, DM, RR, ST, RT, and TT.

MIL 188-114 INTERFACE CONNECTOR PIN ASSIGNMENTS

| Pin # | Mnemonic Name | Direction To DTE | Direction To DCE | Function |
|---|---|---|---|---|
| 1 | | | | Shield |
| 2 | – | | | Not Used |
| 3 | – | | | Not Used |
| 4 | SD | | ⇨ | Send Data A |
| 5 | ST | ⇦ | | Send Timing A |
| 6 | RD | ⇦ | | Receive Data A |
| 7 | RS | | ⇨ | Request to Send A |
| 8 | RT | ⇦ | | Receive Timing A |
| 9 | CS | | | Clear to Send A |
| 10 | – | | | Not Used |
| 11 | DM | ⇦ | | Data Mode A |
| 12 | TR | | ⇨ | Terminal Ready A |
| 13 | RR | ⇦ | | Receiver Ready A |
| 14 | – | | | Not Used |
| 15 | – | | | Not Used |
| 16 | – | | | Not Used |
| 17 | TT | | → | Terminal Timing A |
| 18 | – | ⇦ | | Not Used |
| 19 | SG | | | Signal Ground |
| 20 | RC | ⇦ | | Receive Common |
| 21 | – | | | Not Used |
| 22 | SD | | ⇨ | Send Data B |
| 23 | ST | ⇦ | | Send Timing B |
| 24 | RD | ⇦ | | Receive Data B |
| 25 | RS | | ⇨ | Request to Send B |
| 26 | RT | ⇦ | | Receive Timing B |
| 27 | CS | ⇦ | | Clear to Send B |
| 28 | – | | | Not Used |
| 29 | DM | ⇦ | | Data Mode B |
| 30 | TR | | ⇨ | Terminal Ready B |
| 31 | RR | ⇦ | | Receiver Ready B |
| 32 | – | | | Not Used |
| 33 | – | | | Not Used |
| 34 | – | | | Not Used |
| 35 | TT | | ⇨ | Terminal Timing B |
| 36 | – | | | Not Used |
| 37 | SC | | ⇨ | Send Common |

(Continued)

### Driver Outputs

| | |
|---|---|
| Binary One (Mark), Off | A negative with respect to B |
| Binary Zero (Space), On | A positive with respect to B |
| Driver Impedance (Zout) | 100 ohms or less |
| Output Signal Waveform | With 100 ohms across A and B, the differential signal changes between 0.1 and 0.9 of the pulse width or 20 nanoseconds, whichever is greater |
| Driver Protection | Outputs short circuit protected to ground or to each other (150 mA maximum) |

### Receiver Inputs

| | |
|---|---|
| Binary One (Mark), Off | A negative with respect to B |
| Binary Zero (Space), On | A positive with respect to B |
| Receiver Sensitivity | +/- 200 mV maximum balanced |
| Receiver Impedance (Zin) | 2000 ohms minimum balanced<br>4000 ohms minimum single ended |
| Receiver DC Offset | +/- 7V maximum for proper operation |
| Receiver Protection | +/- 15V maximum without damage to receiver circuits |

### SPECIFICATIONS

| | |
|---|---|
| Dimensions | 5.25" x 4.20" x 0.87"<br>(13.34 cm x 10.67 cm x 2.21 cm) |
| Weight | 7.5 oz (213 gm) |
| Temperature | Operating: 0°C to 50°C<br>(32°F to 122°F) |
| Relative Humidity | 90% maximum, non condensing |

## Introduction

The X.21 interface module provides the data and control signal interface necessary to perform error rate testing in an X.21 environment. Interface drivers and receivers as well as buffers allow the base unit to communicate with an X.21 DCE. The interface signals conform electrically to the X.21 interface specification.

The physical interface of the X.21 interface module is a 15-pin, female, D-type connector.

X.21 INTERFACE CONNECTOR PIN ASSIGNMENTS

| Pin # | Mnemonic Name | Direction To DTE | Direction To DCE | Function |
|---|---|---|---|---|
| 1 | | | | Shield |
| 2 | T (A) | | ⇒ | Transmit |
| 3 | C (A) | | ⇒ | Control |
| 4 | R (A) | ⇐ | | Receive |
| 5 | I (A) | ⇐ | | Indication |
| 6 | S (A) | ⇐ | | Signal Element Timing |
| 7 | B (A) | ⇐ | | Byte Timing |
| 8 | G | | | Signal Ground |
| 9 | T (B) | ⇒ | | Transmit |
| 10 | C (B) | | ⇒ | Control |
| 11 | R (B) | ⇐ | | Receive |
| 12 | I (B) | ⇐ | | Indication |
| 13 | S (B) | ⇐ | | Signal Element Timing |
| 14 | B (B) | ⇐ | | Byte Timing |
| 15 | NOT USED | | | Not Used |

## Interface Signals

**Transmit** – T(A) and T(B) are the differential outputs for transmit data, the Pattern which is selected by the base unit.

**Control** – C(A) and C(B) are the differential outputs representing a control signal. Control in ON whenever the base unit's RTS switch is ON.

**Receive** – R(A) and R(B) are the differential inputs for receive data. Data is received from the DCE as a differential signal, converted to CMOS levels and sent to the base unit for analysis.

**Indication** – I(A) and I(B) are the differential inputs for Indication. The interface merely converts the received signal to levels that are compatible with the base unit. If Indication is ON the LED labeled I will be ON. Otherwise, it will be OFF.

**Signal Element Timing** – S(A) and S(B) are the differential inputs for Signal Element Timing. When timing is received on this circuit, transmit data is generated and output on circuit T. The base unit will always use this timing signal to clock the receive data from circuit R, into the base unit. The LED labeled S will indicate the presence of a clock. The base unit must be set for a Data Rate of External.

**Byte Timing** – B(A) and B(B) are the differential inputs for Byte timing. The interface merely converts the received signal to levels that are compatible with the base unit. If Byte timing is ON the LED labeled B will be ON. Otherwise, it will be OFF.

## Driver Outputs

| | |
|---|---|
| Binary One (Mark), Off | A negative with respect to B |
| Binary Zero (Space), On | A positive with respect to B |
| Driver Impedance (Zout) | 100 ohms max. |
| Rise and Fall Time (10% - 90%) | 20 ns or .1 of the unit interval, whichever is greater. |
| Driver DC Offset | Magnitude: not greater than 3.0V. Magnitude differential: less than 0.4V. |

## Receiver Inputs

| | |
|---|---|
| Binary One (Mark), Off | A negative with respect to B |
| Binary Zero (Space), On | A positive with respect to B |
| Driver Impedance (Zin) | Greater than or equal to 100 ohms |
| Receiver Sensitivity | + / - 300 mV max. |

## SPECIFICATIONS

| | |
|---|---|
| Dimensions | 5.25" L x 4.2" W x 1.17" H (13.33 cm x 10.67 cm x 2.98 cm) |
| Weight | 12 oz. (340 gm) |
| Temperature | Operating: 0°C to 50°C (32°F to 122°F) Storage: -10°C to 55°C (14°F to 131°F) |
| Relative Humidity | 90% maximum, non-condensing |

## 64 KBIT/S G.703 CO-DIRECTIONAL INTERFACE MODULE

The 64 Kbit/s co-directional interface module provides the physical and electrical interface between the base unit and the network under test.

The module consists of a 120 ohm balanced interface via a 25 pin "D" type connector. The module provides for external clock operation only.

The 64 Kbit/s G.703 co-directional interface connector pin assignments are as follows:

| PIN # | DESCRIPTION |
|---|---|
| 2 | TD(A) |
| 14 | TD(B) |
| 3 | RD(A) |
| 16 | RD(B) |

## 8.448 MBIT/S G.703 INTERFACE MODULE

The 8.448 Mbit/s G.703 module provides unframed testing of E2 circuits. The Tx and Rx interface is provided using a 75 ohm unbalanced co-axial connection via BNC connectors.

This module operates using an internal Tx clock only, with a recovered Rx clock.

## SPECIFICATIONS

| | |
|---|---|
| Temperature | Operating: 0°C to 50°C<br>(32°F to 122°F)<br>Storage: -10°C to 55°C<br>(14°F to 131°F) |
| Relative Humidity | 90% maximum, non-condensing |

### Introduction

The DS1/T1 interface module provides the mechanical and electrical interface between the base unit and a T1 type network, allowing bit or block error rate testing, error free second testing, or the analysis of parameters associated with a DS1 signal or a T1-type network. The interface module provides flexibility through front panel slide switch selections to accommodate the majority to T1-type networks. The module's frame format can be either Unframed, D4 ($F_t$), D4 ($F_t$, $F_s$) or ESF. The line code is selectable between either AMI or B8ZS. Transmit timing can be derived from either an internal 1.544 MHz oscillator (Internal) or the recovered receive clock (Loop). The interface module's receiver input impedance can be selected to either TERMINATE or BRIDGE the signal under test.

In addition to transmitting the base unit's data pattern as a DS1 signal and converting the received DS1 signal to clock and data for analysis by the base unit, the interface also monitors the signal for bipolar violations, framing errors, frame sync, CRC errors (ESF only), reception of a Yellow Alarm signal, and the detection of loss of carrier.

### Front Panel Description

The DS1/T1 interface module has four slide switches and a 15-pin, female, D-type connector on its front panel. the top cover Lexan provides the switch labels, as well as the labels for two interface LEDs indicating that SD (Send Data) and RD (Receive Data) are monitored. A thumbscrew located in the center of the module provides a positive mechanical attachment to the base unit. A 37-pin, male, D-type connector is located on the back panel. This connector mates with the connector on the base unit, providing the electrical interface between the two units.

**Framing** – The FRAMING slide switch has four positions and is selectable between UNFRAMED, D4 ($F_t$), D4 ($F_t$, $F_s$) and ESF. Framing, when present, is a bit pattern embedded within the data stream which structures the channelized data for proper retrieval. Depending upon the type of framing, signalling and CRC information may be contained within its structure.

When UNFRAMED, the selected data pattern from the base unit is transmitted without the addition of framing bits.

The D4 ($F_t$) selection provides a modified D4 type framing. The terminal framing ($F_t$) bits are added to the transmitted data stream but the signal framing ($F_s$) bits are not. The receiver only checks the $F_t$ bits to establish frame sync and it ignores the $F_s$ bit positions which are used as data bit positions. This type of framing is used in network applications which use the additional bandwidth for data transmission. (ie. - SLC-96*, digital data only)

The D4 ($F_t$, $F_s$) selection provides true D4 framing, including terminal and signal framing bits, constructed as twelve (12) 193-bit frames to form a Superframe. The receiver checks both $F_t$ and $F_s$ bits to verify frame sync.

The ESF selection provides framing with twenty-four (24) 193-bit frames combined for form and Extended Superframe (Fe).

**B8ZS/AMI** – The B8ZS/AMI switch determines the line code to be used by the module. These two selections basically provide the choice between utilizing zero suppression or not. The user must be aware of the type of line code used on the system under test. If the system uses AMI and the test set has B8ZS selected, the test set will transmit BPVs which may upset network equipment. If the system uses B8ZS and the test set has AMI selected, excess zeroes may be transmitted and intentional bipolar violations will be counted by the test set.

In the B8ZS position, the interface uses the B8ZS (Bipolar with 8 Zero Substitution) method of zero suppression which provides Clear Channel Capability as per the American Telephone and Telegraph Company Compatibility Bulletin 144, Issue 1, April 1981. When B8ZS is selected, the interface transmitter replaces any 8 consecutive zeroes in the transmit data supplied by the base unit with a B8ZS code word (11011000). This code word is transmitted with intentional bipolar violations at bit 4 and bit 7 to distinguish it from ordinary data. The interface receiver recognizes the code word by the bipolar violations and the polarity of the bits. It then converts the code word to 8 zeroes before passing it to the base unit. Although, bipolar violations occur when B8ZS is used, the interface does not recognize them as valid and does not inform the base unit of intentional bipolar violations. Thus, intentional bipolar violations, associated with B8ZS, are not counted by the base unit.

The AMI selection provides the standard Alternate Mark Inversion without zero suppression.

**Internal/Loop Timing** – The transmit timing source is selectable between the INTERNAL 1.544 MHz crystal oscillator or the recovered clock (Loop). In systems slaved to a central timing source, the user must select LOOP TIMING or timing slips will cause errors and sync losses. If a central timing source is not used, a selection of INTERNAL is necessary.

The LOOP selection causes the recovered receive clock to be passed through a jitter attenuator to reduce any jitter produced by the pulsed-tank circuit clock recovery of the interface module receiver. The de-jittered clock is used as the timing source for test set's transmit data.

*SLC is a registered trademark of AT&T.

**Terminate/Bridge** – The TERMINATE/BRIDGE switch changes the input impedance of the interface module receiver. In the TERMINATE position, the receiver input impedance is 100 ohms. This position is used when the test set is terminating the link. The BRIDGE position increases the receiver input impedance to 1k ohms. This position is used for passive monitoring of a network.

**Bipolar Violations (BPV)** – The DS1 signal is an alternate mark inversion signal. This means that a space is zero volts and a mark is a positive or negative pulse. The pulse polarity alternates with each mark. If two consecutive pulses of the same polarity occur, this is a bipolar violation. The DS1/T1 interface module detects these and routes them to the base unit for counting. If B8ZS line coding is selected, bipolar violations caused by B8ZS coding are ignored.

**Framing Errors (FERR)** – Bit errors that occur in the framing word are detected as framing errors and are sent to the base unit for counting and display. Framing errors are only counted by the base unit when a framing format is selected.

**CRC Errors** – The Extended Superframe framing format provides for CRC-6 error checking within its framing bits. The error checking code word is composed of six CRC bits. The transmitter calculates the CRC on the frame being transmitted and transmits the CRC bits in the next frame. The receiver calculates the CRC of a frame being received and compares the calculated CRC word with the CRC word received in the next frame.

The CRC errors detected by the DS1/T1 interface module are sent to the base unit as CRC-6 word errors, not bit errors. Therefore, an ECRC is an Errored CRC word or a frame with bit errors. ECRCs are detected by the interface and passed to the base unit when the framing type is ESF (Extended Superframe).

**Loss of Carrier** – The DS1/T1 interface module continuously monitors the receive signal for activity. If the interface detects thirty-one (31) consecutive zeroes, it indicates to the base unit that there has been a "Loss of Carrier" (Loss of Signal). The base unit, in turn, displays this warning.

**Red Alarm** – Whenever the interface has a framing format other than Unframed selected, it will check the incoming data for frame synchronization by comparing the expected framing pattern with the data stream. Once verified, the unit is in FRAME SYNC. The framing pattern is continuously monitored for frame bit errors after achieving sync. A RED ALARM is declared if 2 out of 5 $F_t$ bits are in error. The base unit will display the message:

RED ALARM
LOST LOCAL FRAME SYNC

**Yellow Alarm** – A Yellow Alarm is a specific, frame-type dependent, bit pattern which is transmitted by network equipment in response to their receiver losing frame synchronization (RED ALARM detection).

The DS1/T1 continuously monitors the incoming data stream for a YELLOW ALARM signal. If the YELLOW ALARM pattern is detected, the base unit is informed and it displays the following message:

YELLOW ALARM
LOST REMOTE FRAME SYNC

## SPECIFICATIONS

| | |
|---|---|
| Specification | AT&T Pub. 62411; AT&T CB144, Issue 1 |
| Signal Format | Bipolar Return-to-Zero |
| Pulse Amplitude | 2.7 to 3.3 volts |
| Pulse Impedance | < .5 dB difference between the total power of the positive and negative pulses |
| Power Level | 12.4 to 18.0 dBm in a 2 kHz band about 772 kHz when transmitting an all-ones pattern |
| Framing Format | Unframed, D4 ($F_t$), D4 ($F_t$, $F_s$), ESF |
| Line Code | AMI, B8ZS |
| Timing Source | Internal, Loop |
| Input Impedance | Terminate (100 ohm), Bridge ( > 1k ohm) |
| Error Detection | Bipolar Violations (BPV), Framing Errors (FERR), CRC Errors (ECRC) |
| Alarms | RED, YELLOW, Loss of Carrier |
| Monitor LEDs | SD, RD |
| Speed | 1.544 MHz |
| Connector | 15-pin, female, D-type (standard)<br>15-pin gender changer (standard)<br>15-pin D-type to 310 (optional)<br>15-pin D-type to bantam (optional) |
| Dimensions | 5.25" x 4.20" x 1.17"<br>(13.34 cm x 10.67 cm x 2.99 cm) |
| Weight | 10 oz. (283 gm) |
| Temperature: | Operating: 0°C to 50° C<br>(32°F to 122°F) |
| Relative Humidity | 90% non-condensing |

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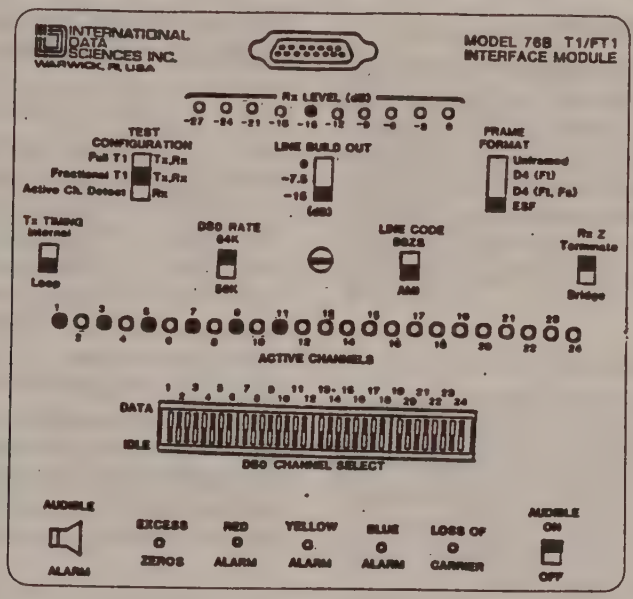



T1/FRACTIONAL T1 FRONT PANEL LINE DRAWING

### Introduction

The T1/Fractional T1 interface module plugs into the IDS Bit Error Rate Test Set base units listed on cover page and provides the user with the ability to perform error rate testing on full T1 circuits as well as fractional T1 circuits. This module also allows the user to monitor an incoming T1 signal and determine which channels of the framed signal contain data and which contain idle characters.

The T1/Fractional T1 interface module provides selections for the Test Configuration, Line Build-Out, Frame Format, Tx Timing Source, DS0 Rate, Line Code, Rx Impedance, Individual Channel Content, and Audible Alarm Enable. Both contiguous and non-contiguous fractional T1 circuits can be tested at channel rates of 56 Kbps or 64 Kbps.

In the Fractional T1 mode, each of the 24 channels can be directed by the user to transmit either a Data or an Idle code. The test set then transmits the selected data pattern in each of the channels selected to contain data. The interface then transmits the framed 1.544 MHz T1 signal consisting of the selected data channels containing the test pattern and the channels containing the idle codes. The receiver performs an error rate test on the test pattern in the selected Data channels.

Twenty-four channel LEDs provide an indication of either the channels currently being used to transmit and/or receive a test pattern, or the Data/Idle status of the channels in a received framed T1 signal. Five LEDs provide a visual indication of a Red, Yellow, or Blue Alarm, Loss of Carrier or Excess Zeros. An audio tone occurs at half second intervals, if enabled, when an alarm is active. Ten LEDs provide a moving dot dB meter which constantly monitors the receive signal.

### Front Panel Description

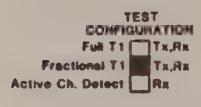
#### T1/Fractional T1 Connector

This 15-pin, female, D-type connector provides the physical interface connection to the T1 circuit. Adapters are available for connection to 310, bantam, and RJ45 jacks.

#### Rx Level (dB) Meter

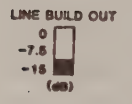
Ten red LEDs form a moving dot dB meter which provides a general indication of the receive level at the interface. It has a range of -27 dB to 0 dB, in 3 dB increments. The dB meter measures signal power not pulse power. Therefore, the dB readings are pattern sensitive and should be done with a mark, if possible, for the greatest accuracy. Random data will generally give a reading that is 3 to 6 dB lower. Whenever the signal level is above -27 dB, one of the LEDs will be lit. The receive signal level is at least the dB level indicated by the lit LED, but less than the next higher level or more positive LED value (the LED to the right of the LED which is on).

### Test Configuration




This three-position slide switch allows the user to transmit and receive/analyze a Full T1 signal, a Fractional T1 signal with user-selectable data channels, or in the Active Channel Detect position, to automatically detect which received T1 channels contain data and which contain idle characters.

### Line Build-Out




This three-position slide switch allows the selection of three levels of line build-out: 0 dB, -7.5 dB and -15 dB. The -7.5 dB and the -15 dB positions provide output signals which are equivalent to the output of cables having 7.5 dB and 15 dB losses, respectively.

### Frame Format

This four-position slide switch allows the selection of either unframed data, D4 (with $F_t$ bits only) framing format, D4 (with both $F_t$ and $F_s$ bits) framing format or Extended Superframe (ESF) format. In the Unframed mode, data is transmitted as a continuous bit stream without the addition of framing bits. In the framed modes, a bit pattern embedded within the data stream structures the channelized data for proper retrieval.

The D4 ($F_t$) selection provides a modified D4 type framing. The terminal framing ($F_t$) bits are added to the transmitted data stream, but the signal framing ($F_s$) bits are not. The receiver checks the $F_t$ bits to establish frame sync and ignores the $F_s$ bit positions which are used as data bit positions. This type of framing is used in network applications which use the additional bandwidth for data transmission such as SLC-96*. (SLC is a registered trademark of AT&T)

The D4 ($F_t$, $F_s$) selection provides data which is formatted with conventional D4 framing, utilizing six terminal framing bits ($F_t$) and six signal framing bits ($F_s$) to qualify and maintain frame synchronization. The $F_s$ bits identify the frames containing signalling information. This framing type consists of twelve 193-bit frames combined to form a Superframe.

The ESF selection provides framing which consists of twenty-four 193-bit frames combined to form an Extended Superframe (Fe). ESF uses only six framing bits which perform the functions of both the $F_t$ and $F_s$ bits of D4. Six additional bits are used for CRC or error checking and twelve bits are available for a data link. When testing an ESF signal, the CRC is monitored for errors and the data link bits will contain test pattern bits.

### Tx Timing

This two-position slide switch allows the transmit timing source to be selectable between either the INTERNAL 1.544 MHZ crystal oscillator or the recovered clock (LOOP). In systems slaved to a central timing source, the user must select LOOP TIMING or timing slips will cause errors and sync losses. If a central timing source is not used, then a selection of INTERNAL is necessary. The LOOP selection causes the recovered receive clock to be passed through a jitter attenuator to reduce any jitter produced by the pulsed-tank circuit clock recovery of the interface module receiver. The de-jittered clock is used as the timing source for the test set's transmit data.

### DS0 Rate

This two-position slide switch allows the user to choose an effective channel rate of either 56K or 64K, depending upon the network requirement. When 64K is selected, all eight bits of a data channel contain pattern data, providing clear channel capability. When 56K is selected, only seven bits in each active channel contain data. The eighth bit is always a one. Whenever the Frame Format selection is Unframed, the interface will default to 64K, regardless of the DS0 Rate selection.

### Line Code

This two-position slide switch determines the line code to be used by the module. Basically, the two selections provide the choice between utilizing zero suppression or not. If the system uses AMI and the test set has B8ZS selected, the test set will transmit BPVs which may upset network equipment. If the system used B8ZS and the test set has AMI selected, excess zeroes may be transmitted and the intentional bipolar violations will be counted by the test set.

In the B8ZS position, the interface uses the B8ZS (Bipolar with 8 Zero Substitution) method of zero suppression which provides Clear Channel Capability as per the AT&T Compatibility Bulletin 144, Issue 1, April 1981. When B8ZS is selected, the interface transmitter replaces any 8 consecutive zeros in the transmit data supplied by the base unit with a B8ZS code word (11011000). This code word is transmitted with intentional bipolar violations at bit 4 and bit 7 to distinguish it from ordinary data. The interface receiver recognizes the code word by the bipolar violations and the polarity of the bits. It then converts the

code word to 8 zeros before passing it to the base unit. Although bipolar violations occur when B8ZS is used, the interface does not recognize them as valid and does not inform the base unit of intentional bipolar violations. Thus, intentional bipolar violations are not counted by the base unit when B8ZS is selected. The AMI selection provides the standard Alternate Mark Inversion without zero suppression. It should be noted that if AMI is selected with framed data, zero suppression will effectively occur when a DS0 Rate of 56K is selected because the eighth bit of every channel is forced to a one.

### Rx Impedance

This two-position slide switch changes the input impedance of the receiver. In the TERMINATE position, the receiver input impedance is 100 ohms. This position is used when the test set is terminating the link. The BRIDGE position increases the receiver input impedance to 1K ohms. This position is used for passive monitoring of a network.

### DS0 Channel Select

Twenty-four dip switches labeled DS0 CHANNEL SELECT are used in the Fractional T1 test configuration to select which channels are to contain the test pattern data and which are to contain idle characters for transmission within the T1 frame. The receiver will only look at the channels selected as DATA for analysis of the received data. Each channel switch is numbered according to its respective channel position within the frame. Each switch has two selectable positions labeled DATA and IDLE. When a channel select switch is "on" (DATA position), the appropriate active channel LED will light and 7 or 8 bits of the selected transmit data pattern, depending upon the DS0 Rate selection, are placed in that channel of each frame. When a switch is "off" (IDLE), the LED associated with that channel will be "off," and an idle code of 7FH will be transmitted in that channel of each frame.

### Active Channels LEDS

Twenty-four green LEDs labeled ACTIVE CHANNELS are provided to inform the user which channels of the frame contain data and which contain idle codes. When the Active Channel Detect test configuration is selected, the receiver will examine each channel for repetitive data. If the data within a channel is repetitive, the test set assumes the presence of an idle code and turns "off" the LED associated with that channel. If the channel data is non-repetitive, the test set assumes the presence of true data and turns "on" the LED associated with that channel.

In the Fractional T1 test configuration, each channel LED will indicate whether its respective DS0 Channel Select switch is in the DATA position (LED "on") or in the IDLE position (LED "off"). In the Full T1 test configuration, all of the Active Channel LEDs will be "on," indicating that all channels are being used for the selected test pattern. If unframed data is selected when the test configuration is either Fractional T1 or Active Channel Detect, the active channel LEDs will flash at a one second rate and the audio alarm will sound, if enabled, to tell the user to select a framed format.

### Audible Alarm

When enabled by the AUDIBLE On/Off switch, this speaker generates an audible tone whenever a RED, YELLOW, BLUE, LOSS OF CARRIER or EXCESS ZEROS ALARM is detected. The tone will turn "on" and "off" at a one second rate and will continue as long as any alarm condition exists.

### Excess Zeros LED

The T1/FT1 Interface Module monitors the incoming signal for an excessive number of consecutive zeros. The number of consecutive zeros required to cause an Excess Zeros indication is determined by the Line Code selection. When the Line Code is B8ZS, any 8 consecutive zeros, including framing bits, will cause the EXCESS ZEROS LED to light for a minimum of two seconds and the audio alarm to sound, if enabled. When the Line Code selection is AMI, 16 consecutive zeros, including framing bits, are required to cause an EXCESS ZEROS alarm indication.

### Red Alarm LED

Whenever the interface has a framing format other than Unframed selected, it will check the incoming data for frame synchronization by comparing the expected framing pattern with the data stream. Once verified, the unit is in FRAME SYNC. The framing pattern is continuously monitored for frame bit errors after achieving

sync. The RED ALARM LED is turned "on" if 2 out of 5 of the F bits are in error. The Audible Alarm will also sound, if enabled. When in the Full or Fractional T1 test configurations, the base unit will also display the message:

RED ALARM
LOST LOCAL FRAME SYNC

### Yellow Alarm LED

A YELLOW ALARM is a specific, frame-type dependent bit pattern which is transmitted by network equipment in response to their receiver losing frame synchronization (RED ALARM detection). In the D4 ($F_t$) and D4 ($F_t$, $T_s$) framing formats, a yellow alarm is declared if bit 2 of all channels is a 0 for 256 or more consecutive channels.

In the ESF format, a yellow alarm is declared if a repeating pattern of 00FFH is detected for sixteen repetitions. The T1/Fractional T1 Interface Module continuously monitors the incoming data stream for a YELLOW ALARM signal. If the YELLOW ALARM pattern is detected, the YELLOW ALARM LED is turned "on" and the Audible Alarm will sound, if enabled. The base unit will display the following message if the interface is not in the Auto Channel Detect configuration:

YELLOW ALARM
LOST REMOTE FRAME SYNC

### Blue Alarm LED

The T1/Fractional T1 Interface Module monitors the incoming data stream for an AIS (Alarm Indication Signal). A Blue Alarm is declared whenever 2 consecutive frames contain less than 3 zeros within the channel data. Upon detection, the BLUE ALARM LED is turned "on" and Audible Alarm will sound, if enabled. A Blue Alarm indicates that a transmission fault has occurred upstream. It is transmitted by the one detecting the fault in order to maintain network timing integrity. No message is displayed on the base unit.

### Loss of Carrier LED

The T1/Fractional T1 Interface Module continuously monitors the receive signal for data activity. If the receiver detects thirty-two consecutive zeros, the LOSS OF CARRIER LED is turned "on" and the Audible Alarm will sound, if enabled. A Loss of Carrier alarm takes precedence over the other alarms by the base unit. Therefore, even though a Red Alarm LED may also be "on," the base unit will display "LOSS OF CARRIER" on its LCD. Note: The base unit will not display any error message when in the Auto Channel Detect configuration.

### Audible On/Off

This two-position slide switch enables or disables the Audible Alarm.

## OPERATION

The T1/Fractional T1 (T1/FT1) Interface Module for the IDS BERT test sets provides the physical interface to the network via a 15-pin, female, D connector. Adapters are available for 15-pin to 310 plugs, 15-pin to bantam plugs, and 15-pin to RJ45 connectors. This interface is capable of testing full or fractional T1 networks, and providing the means to select a variety of T1 format variables such as FRAME FORMAT, LINE CODE, amount of LINE BUILD-OUT, the effective channel rate (DS0 RATE), the Tx TIMING source and the IMPEDANCE.

The proper switch selections must be made in any of the test configuration modes in order to match the T1/Fractional T1 Interface Mode parameters to the parameters of the T1 network under test. The only restriction is that the Unframed format cannot be selected when the test configuration is either Fractional T1 or Active Channel Detect. These modes require channelization which is only possible in a framed T1 signal. If Unframed is selected in either of these modes, the 24 Active Channel LEDs will flash at a one second rate to indicate to the user to select a frame format.

At power-up the unit will turn the 24 channel LEDs, the 5 alarm LEDs and the audio (if enabled) "on" for approximately 4 seconds. The interface module's program memory is tested during this time. If there is program memory failure, the 5 alarm LEDs will flash and the audio (if enabled) will sound.

The interface module is internally reset whenever an interface switch is changed, however, the base unit should also be reset anytime an interface switch has been changed in order to avoid the display of erroneous data.

LOOP UP/LOOP DOWN codes may be initiated by the base unit. The interface must be in the Full T1 configuration.

If the base unit is a Model 77, no restrictions apply. However the Model 76B must have a pattern selection other than Mark. If two Model 76Bs are set up in a full duplex arrangement and either a LOOP UP or LOOP

DOWN is performed, the results will be erroneous if they both have the same pattern selected. This is because the Model 76B does not have the ability to look at the loop pattern bit for bit. It only looks for synchronization of the selected pseudo-random pattern after the loop pattern has been transmitted for its specified time. If the patterns are the same, it may think it has looped up when it has not, or that it has not looped down when it actually has.

The 1 in 8 and the 3 in 24 pattern selections on the base unit are intended to be used to stress the network by placing the maximum number of allowable zeros in the data field. In order to utilize the patterns effectively, they should only be used when the DS0 Rate is 64K. At this time, the true channelized 1 in 8 or 3 in 24 test pattern is transmitted. If the DS0 Rate selection is 56K, only 7 bits of the pattern will be placed in a channel because bit 8 is forced to a one. The intended eighth pattern bit is placed in the next data channel, thus shifting the stress pattern. The stress patterns will still achieve synchronization and not trigger alarms when operating with 56K channels, however, they will not align on a channel basis and will not stress the network because it is already limited to a maximum of 7 zeros by the DS0 selection.

### Full T1

The Full T1 test configuration allows the user to test either framed or unframed T1 signals which utilize the full bandwidth available for data transmission. For unframed T1, this means a full 1.544 MHz bandwidth for data. For framed T1 with 64K channels, all 24 channels are used for data transmission providing an effective bandwidth of 1.536 Mhz for data and a bandwidth of 8 kHz for framing. For framed T1 with 56K channels, the bandwidth is 1.344 MHz for data, 8 kHz for framing and 192 kHz for the eighth bit of every channel being a "one."

When the Full T1 test configuration is selected, the 24 Active Channel LEDs light, indicating that the test pattern selected on the base unit will be transmitted and received in all 24 channels of every frame. The user must select the proper Frame Format, Line Build-Out, Tx Timing source, DS0 Rate, Line Code and Receiver Termination.

Bipolar violations, framing errors and CRC errors are sent to the base unit for counting these events. Alarm conditions are reported by LEDs on the module. Loss of Carrier, Red Alarm, and Yellow Alarm messages are displayed on the LCD of the base unit. An audible alarm can be enabled to indicate an alarm condition. A ten LED Rx level meter located just below the 15-Pin D connector provides a general indication of the received signal power.

### Fractional T1

The Fractional T1 test configuration allows the user to make the same selections as Full T1, except that the Frame Format must not be Unframed. With Fractional T1, the bandwidth available for user data is determined by the number of 56 or 64 kHz channels leased. The channels not containing data must contain an idle code. If a user has leased a one quarter T1 link and used 64 kHz channels, 6 channels (24 divided by 4) would be available and the effective bandwidth would be 384 kHz (64K times 6). If 56 kHz channels are used, the effective bandwidth for data would be 336 kHz (56K times 6). Data channels may be either contiguous or non-contiguous.

Contiguous channels are a group of consecutive channels utilized for data transmission, such as channels 1, 2, 3, 4, 5 and 6. This Fractional T1 channelization requires the user to adhere to minimum pulse density requirements. This can be achieved by using either 56 kHz channels in which bit 8 of each channel is a 1 or by using 64 kHz channels with B8ZS Clear Channel Capability.

Non-contiguous channels are alternate channels in a frame, such as 1, 3, 5, 7, 9 and 11. They are required when operating with an AMI line code and 64 kHz channels in order to ensure a minimum pulse density. This is maintained by having an idle character in every other channel.

When in the Fractional T1 configuration, 24 dip switches allow the user to select which channels will contain data and which channels will contain a 7FH idle code within a transmitted frame. The same channels selected as DATA are analyzed by the receiver for the selected test pattern. The 24 Active Channel LEDs provide a visual display of the channel switch selections where the respective channel LED is "on" for DATA and "off" for an IDLE code.

The pattern selected by the base unit is transmitted serially in the selected DATA channels and a 7FH IDLE code is transmitted in each of the other channels. The receiver drops the selected DATA channels from the received frames and sends the data to the base unit for pattern analysis at the effective bandwidth rate. The overall T1 frame is analyzed by the interface for alarm conditions and T1 associated errors.

In non-contiguous T1, the data may come back with one or more channels delayed due to different routing paths through the network. If this occurs, the base unit will not sync up with a pseudo-random pattern selected. However it will sync up with a Mark when the DS0 Rate is 56K or a Mark, Alternate or a 1 in 8 pattern when the DS0 Rate is 64K. This is because these patterns are repetitive on a channel basis and will be consistent regardless of any delayed channels. In order to test non-contiguous with a pseudo-random pattern, the user would have to perform the test on each individual channel.

### Active Channel Detect

The Active Channel Detect test configuration selection provides the user with the ability to determine which chan-

nels of a Fractional T1 link are being utilized for data transmission and which channels are idle. The same Full T1 setup selections are allowed except the signal must be framed. In the Active Channel Detect configuration, the Receiver monitors each channel of a framed T1 signal for either changing data or repetitive data.

The twenty-four channel LEDs will inform the user of channel content. If a channel contains variable data, its respective LED will be "on." If a channel contains a repetitive byte, it is considered idle and the respective LED will be "off." The interface transmitter continuously transmits idle characters in each channel while in this mode, and if looped back to its receiver, all of the channel LEDs would be "off."

## SPECIFICATIONS

| | |
|---|---|
| Configurations | Full T1, Fractional T1<br>Active Channel Detect |
| Framing Format | Unframed, D4 ($F_t$), D4 ($F_t$, $F_s$), ESF |
| Line Code | B8ZS, AMI |
| Channel Rate | 56 kHz, 64 kHz |
| Rx Impedance | Terminate (100 ohms)<br>Bridge ( > 1 k ohms) |
| Line Build Out | 0 dB, -7.5 dB, -15 dB |
| Tx Timing | Internal (1.544 MHz crystal)<br>Loop (recovered receive clock) |
| Rx Level Meter | Ten (10) red LEDs<br>0 to -27 dB (3 dB increments) |
| Channel LEDs | Twenty-four (24) green LEDs<br>(Ch. 1-24)<br>Indicates all 24 channels are used for data in the Full T1 Test Config.<br>Indicates position of 24 channel switches in Fractional T1 Test Config.<br>Indicates channel contents (data or idle) in Active Channel Detect Test Configuration<br>Data indication - LED "on"<br>Idle indication - LED "off" |
| Ch. Select Switches | Twenty-four (24) dip switches<br>Selects channel contents (Data or Idle) in Fractional T1 Test Configuration |
| Alarm LEDs | EXCESS ZEROS Alarm (yellow)<br>RED Alarm (red)<br>YELLOW Alarm (yellow)<br>BLUE Alarm (red)<br>LOSS OF CARRIER Alarm (yellow) |
| Audible Alarm | Activated for alarm conditions, an Unframed selection (Fractional T1 or Auto Channel Detect) or a program memory failure detected at power up.<br>Approximately 5 kHz tone alternating "on" and "off" at one half second intervals<br>Audible Enable switch selectable |
| Enclosure | Plastic Molded |
| Dimensions | 5.95" L x 5.60"W x 1.75"D |
| Weight | 1.5 lbs. |
| Temperature | Operating: 0°c to 50° C<br>(+32° F to +122° F)<br>Storage: -20°C to +70° C<br>(-4° F to +150° F) |
| Humidity | 90% maximum (non-condensing) |

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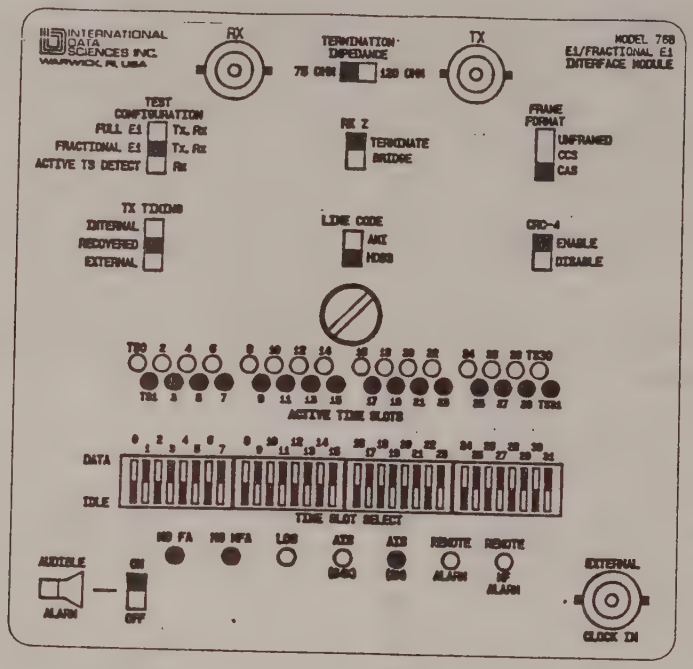



E1/FRACTIONAL E1 FRONT PANEL LINE DRAWING

## Introduction

The E1/Fractional E1 Interface Module, for use with IDS Bit Error Rate Test sets listed on front cover, provides the physical interface to the network via BNC connectors. This interface, capable of testing full or fractional E1 networks, provides flexibility in selecting E1 format variables. These are Frame Format, CRC-4, Line Code, the Tx Timing source, and Impedance.

The proper switch selections must be made in order to match the E1/Fractional E1 Interface Module parameters to the parameters of the E1 network under test. The only restriction is that the Unframed format cannot be selected when the Test Configuration is either Fractional E1 or Active TS Detect because framing is required for defined time slots to exist.

If Unframed is selected in either of these modes, the 32 Active Time Slot LEDs will flash at a one second rate and the audio alarm will sound, if enabled, until the setup error is corrected.

At power-up, the unit will turn the 32 time slot LEDs, the 7 fault LEDs, and the audio (if enabled) "on" for approximately 4 seconds. The interface module's program memory is tested during this time. If there is a program memory failure, the 7 fault LEDs will flash and the audio will sound. The interface module is internally reset whenever an interface switch is changed. In order to avoid the display of erroneous data, the base unit should also be Reset anytime an interface switch has been changed

## Operation

**Full E1** – The Full E1 Test Configuration allows the user to test either framed or unframed E1 signals which utilize the full bandwidth available for data transmission. When the Full E1 test configuration is selected, and the Frame Format selection is Unframed, all of the Active Time Slot LEDs will be lit, indicating that the entire bandwidth is being utilized for data transmission.

When the Frame Format selection is CCS, the TS0 LED is "off," indicating that it contains the frame alignment signal, and the TS1-TS31 LEDs will be "on," indicating that data is to be transmitted and received in those channels.

When the Frame Format selection is CAS, TS0 and TS16 LEDs are "off" because they contain the frame and multiframe alignment signals, respectively, and the Active Time Slot LEDs for TS1-TS15 and TS17-TS31 are "on" because they are available for data transmission.

The user must select the proper Frame Format, Tx Timing source, Line Code, Impedance and Receiver Termination. Bipolar violations, framing errors, and CRC errors are sent to the base unit for counting these events. Alarm and fault conditions are reported by LEDs on the module. An audible alarm can be enabled to indicate an alarm or fault condition.

**Fractional E1** – The Fractional E1 Test Configuration allows the user to make the same selections as Full E1, except that the Frame Format must not be Unframed.

With fractional E1, the bandwidth available for user data is determined by the number of time slots leased. The time slots not containing data will contain all 1's.

When in the Fractional E1 Configuration, the user is allowed to select which time slots will contain data and which time slots will contain the idle code (11111111) within a transmitted frame.

The same time slots selected as DATA are analyzed by the receiver for the selected test pattern. Although there are 32 dip switches, representing the 32 time slots of a frame, the Time Slot 0 switch has no effect because the frame alignment signal is always in TS0. The Time Slot 16 switch only has an effect when the framing is CCS. When the framing is CAS, the TS16 switch has no effect because the multiframe alignment signal is in TS16.

The 32 Active Time Slot LEDs provide a visual display of the time slot switch selections, where the respective time slot LED is "on" for DATA and "off" for an IDLE code. The time slots which should contain the frame and multiframe alignment signals (TS0 and TS16) are indicated by their respective time slot LEDs being "off."

The pattern selected by the base unit is transmitted serially in the selected DATA time slots, and the IDLE code is transmitted in each of the other time slots. The receiver drops the selected DATA time slots from the received frames and sends the data to the base unit for pattern analysis at the effective bandwidth rate. The overall E1 frame is analyzed by the interface for errors, as well as, alarm and fault conditions.

**Active TS Detect** – The Active Time Slot Detect Test Configuration selection provides the user the ability to determine which channels of a fractional E1 link are being utilized for data transmission and which channels are idle. The same Full E1 setup selections are allowed, except that the signal must be framed. In the Active TS Detect Configuration, the receiver monitors each non-framing related time slot of a framed E1 signal for all 1's, indicating an idle time slot. The 32 Time Slot LEDs will inform the user of time slot content.

If a time slot contains all 1's, its respective LED will be "off" and if it contains data other than a mark, its respective LED will be "on." The TS0 LED will always be "off," because time slot 0 contains the frame alignment signal. The TS16 LED will be "off" if the framing is CAS, indicating that TS16 is used for the multiframe alignment signal. The interface transmitter is still active in this mode and transmits pattern DATA in the time slots selected by the Time Slot Select switches. If looped back to the receiver, the time slot LEDs would be "on" for those containing data and "off" for those containing all 1's.

The E1/Fractional E1 Interface Module plugs into the base unit and allows the user to perform error rate testing on full E1 (2.048 MHz) circuits, as well as, fractional E1 circuits. It also allows the user to monitor an incoming E1 signal and determine which time slots of the framed signal contain data and which contain an all 1's idle character.

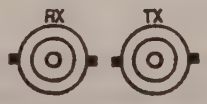
The interface module provides selections for the Test Configuration, Line Code, Frame Format, CRC-4, Tx Timing Source, Impedance, Rx Z, Individual Time Slot content, and Audible Enable. In the Fractional E1 mode, TS1-TS15 and TS17-31 are always selectable to be either data or the idle code. TS16 is also available for Data/Idle characters when the framing format is CCS. The test set provides the selected data pattern at the effective rate of the bandwidth required by the number of time slots selected as data.

The interface transmits the framed 2.048 MHz E1 signal, which consists of the selected data time slots containing the test pattern and the time slots with the idle code inserted. The receiver removes the test pattern from the selected Data time slots and performs an error rate test on it.

Thirty-two Time Slot LEDs provide an indication of either the time slots currently being used to transmit and/or receive a test pattern or the Data/Idle status of the channels in a received framed E1 signal. Seven LEDs provide a visual indication of No Frame Alignment (FA), No Multiframe Alignment (MFA), Loss of Signal, AIS (64K), AIS (2M), Remote Alarm, and Remote Multiframe Alarm. An audio tone occurs at half second intervals, if enabled, when any of the fault LEDs are lit.

## FRONT PANEL DESCRIPTION

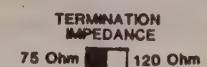
### E1/Fractional E1 Connectors




The physical interface connection to the E1 circuit is provided by BNC connectors.

## SWITCHES

### Impedance



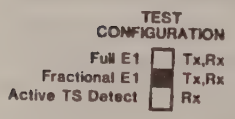

This two-position slide switch changes the impedance of both the transmitter and receiver. In the 75 ohm position, impedance is 75 ohms and in the 120 ohm position, impedance is 120 ohms.

### Rx Z

This two-position slide switch determines whether the receiver input impedance is the value selected by the Im-

pedance switch (TERMINATE) or an impedance greater than 1K ohms (BRIDGE).

### Test Configuration




This three-position slide switch allows the user the ability to transmit and receive/analyze a FULL E1 signal, a FRACTIONAL E1 signal with user-selectable data time slots or in the ACTIVE TS DETECT position, to automatically detect which received E1 time slots contain data and which contain the idle character.

### Frame Format

This three-position slide switch allows the selection of either unframed data, CCS (Common Channel Signalling) frame format or CAS (Channel Associated Signalling) multiframe format. In the Unframed format, data is transmitted as a continuous bit stream without the addition of framing bits. In the framed modes, a bit pattern, embedded within the data stream, structures the signal into time slots for proper data retrieval.

The CCS or Common Channel Signalling format utilizes time slot 0 for frame alignment but has no multiframe alignment. Time slot 16 will be used for pattern data when Full E1, or selectable as Data or an all 1's Idle code when Fractional E1.

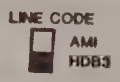
The CAS or Common Associated Signalling format utilizes time slot 0 for frame alignment and time slot 16 for multiframe alignment.

### Tx Timing

This three-position slide switch allows the transmit timing source to be selectable between either the INTERNAL 2.048 MHz. crystal oscillator, the RECOVERED clock, or an EXTERNAL clock. In systems slaved to a central timing source, the user must select RECOVERED Tx Timing or timing slips will cause errors and sync losses. If a central timing source is not used, then a selection of either INTERNAL or EXTERNAL may be used.

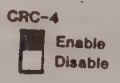
The RECOVERED selection causes the recovered clock to be passed through a jitter attenuator to reduce any jitter produced by the pulsed-tank circuit clock recovery of the interface module receiver. The de-jittered clock is used as the timing source for the test set's transmit data. In the EXTERNAL position, no de-jitter circuitry is used and the quality and tolerance of the clock is dependent upon the external clock source.

### Line Code




This two-position slide switch determines the line code to be used by the module. In the AMI position, the signal is a standard alternate mark inversion coding scheme with no zero suppression. In the HDB3 position, zero suppression is accomplished with HDB3 (high density bipolar order of 3) encoding.

### CRC-4




This two-position slide switch allows the user to enable or disable the CRC-4 (CYCLIC REDUNDANCY CHECK-4) multiframe format. The CRC-4 format utilizes bit 1 of time slot 0 for CRC-4 alignment. This switch is ignored whenever the Frame Format selection is Unframed.

### Active Time Slots (LEDs)

Thirty-two green LEDs, labeled ACTIVE TIME SLOTS, are provided to inform the user as to which time slots of the frame contain data and which contain an all 1's idle code.

Whenever unframed full E1 is selected, all of the Active Time Slot LEDs will be "on," indicating that all time slots are being used for the selected test pattern. If CCS framing is selected, the TS0 LED will go "off," indicating that time slot 0 is being used for the frame alignment signal and not the selected test pattern. If CAS framing is selected, the TS16 LED will also be "off," indicating that time slot 16 is being used for the multiframe alignment signal and not the selected test pattern.

In the Fractional E1 test configuration, each Time Slot LED will indicate whether its respective Time Slot Select switch is in the DATA position (LED "on") or IDLE position (LED "off"). The TS0 LED will always be "off." The TS16 LED will be "off" if the framing is CAS, otherwise, it will indicate if Data or Idle is selected for time slot 16.

When the Active TX Detect test configuration is selected, the receiver will examine each time slot for an all 1's Idle code. If the Idle code is detected, the test set turns "off" the LED associated with that time slot. If the Idle code is not detected in a time slot, the test set turns "on" the LED associated with the time slot. The TS0 LED will always be "off" and the TS16 LED will also be "off," if CAS framing is selected.

### Time Slot Select

Thirty-two dip switches, labeled TIME SLOT SELECT, are used in the Fractional E1 test configuration to select which time slots are to contain the test pattern data and which are to contain idle characters for transmission within the E1 frame. The receiver will only look at the time slots selected as DATA for analysis of the received data. Each time slot switch is numbered according to its respective time slot position within the frame. Each switch has two selectable positions labeled DATA and IDLE.

When a time slot select switch is "on" (DATA position), the appropriate active time slot LED will light and 8 bits of the selected transmit data pattern are placed in that time slot of each frame. When a switch is "off" (IDLE), the LED associated with that channel will be "off" and the idle code (11111111) will be transmitted in that channel of each frame.

Time slot 0 switch has no effect because the frame alignment signal is located there. Time slot 16 is only available for selection when the framing is CCS. When the framing selection is CAS, time slot 16 contains the multiframe alignment signal, therefore, the TS16 switch position is ignored.

### No FA LED

This red LED indicates that the test set's receiver has either lost or never achieved Frame Alignment.

### No MFA LED

This red LED indicates that the test set's receiver has either lost or has never achieved Multiframe Alignment.

### Loss Of Signal LED

This red LED indicates that the receiver has received at least 32 consecutive zeros and declared a loss of signal condition.

### AIS (64K) LED

This red LED turns "on" when the contents of time slot 16 have been an all "ones" signal for at least two consecutive frames.

### AIS (2 M) LED

This red LED turns "on" when less than 3 bit positions in the last FAS and non-FAS frames received are a 0.

### Remote Alarm LED

The Remote Alarm LED indicates that a remote alarm has been detected and that remote frame alignment has been lost. It is declared when bit 3 of time slot 0 in non-FAS frames is a "1" for three consecutive non-FAS frames.

### Remote MF Alarm

The Remote MF Alarm LED indicates that remote alarm has been detected and that remote multiframe alignment has been lost. It is declared whenever bit 6 of time slot 16 in frame 0 is a "1" for three consecutive multiframes.

### Audible Alarm

When enabled by the AUDIBLE On/Off switch, this speaker generates an audible tone whenever a fault or alarm is detected. The tone will turn "on" and "off" at a one second rate and will continue as long as any alarm conditions exists.

### Audible On/Off

This two-position slide switch enables or disables the Audible Alarm.

### External Clock In

This BNC connector, in conjunction with the Tx Timing switch, provides the user with the ability to transmit the test set patterns using an external 0 to 5V squarewave timing source.

## SPECIFICATIONS

| | |
|---|---|
| Test Configurations | Full E1, Fractional E1, Active TS Detect |
| Framing Format | Unframed, CCS, CAS |
| CRC-4 | Enable/Disable |
| Line Code | HDB3, AMI |
| Termination Z | 75 ohms, 120 ohms |
| Rx Z | Terminate<br>Bridge (>1 k ohms) |
| Tx Timing | Internal (2.048 MHz crystal)<br>Recovered (from receive data)<br>External (BNC 0-5V input) |
| Time Slot LEDs | Thirty-two (32) green LEDs (TS 0-31) |
| | Indicates data time slots in the Full E1 Test Configuration |
| | Indicates position of 32 time slot switches in Fractional E1 Test Configuration |
| | Indicates time slot contents (non-Mark Pattern DATA or all 1's, if IDLE) in Active TS Detect Test Configuration |
| | Data (non-Mark) – LED "on"<br>Idle (all 1's) – LED "off" |
| | CCS Framing – TS0 LED "off" |
| | CAS Framing – TS0 and TS16 LEDs "off" |
| TS Select Switches | Thirty-two (32) dip switches<br>Selects time slot contents for TS1-15 and TS17-31 if Framed Fractional E1 Test |
| | DATA – Pattern data (nom-Mark)<br>IDLE – All 1's (11111111) |
| Fault & Alarm LEDs | NO FA LED<br>NO MFA LED<br>LOSS OF SIGNAL LED<br>AIS (64K) LED<br>AIS (2M) LED<br>REMOTE ALARM LED<br>REMOTE MF ALARM LED |
| Audible Alarm | Approximately 5 kHz. tone alternating "on" and "off" at one half second intervals |
| | Audible Enable - switch selectable |
| | Activated:<br>Alarm and fault conditions |
| | Unframed (Fractional E1 or Active TS Detect) |
| | Program memory failure at power up |
| Enclosure | Plastic molded |
| Dimensions | 5.95" L x 5.60" W x 1.75" D |
| Weight | 1.5 lbs. |
| Temperature | Operating: 0° to 50° C (+32° F to +122°F)<br>Storage: -20° to +70° C (-4° F to +150° F) |
| Humidity | 90% maximum (non-condensing) |

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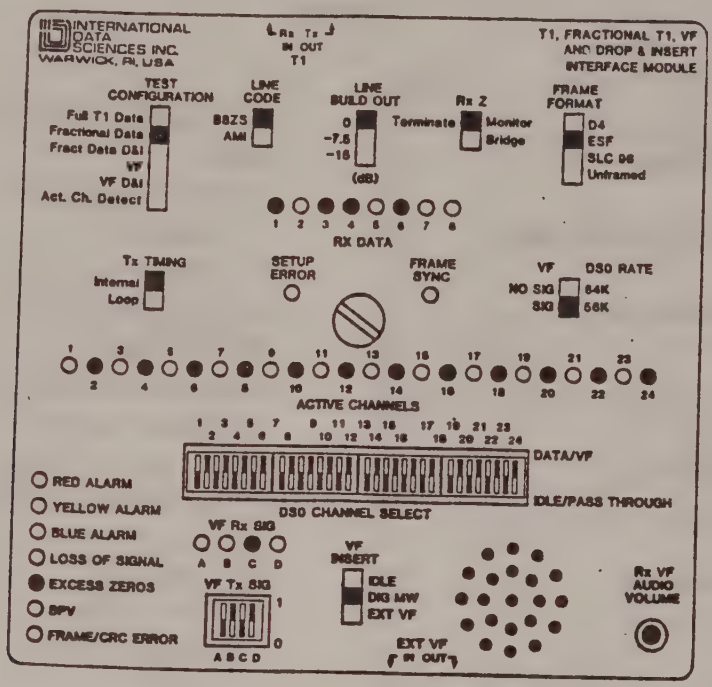



T1/FRACTIONAL T1, VF AND DROP AND INSERT FRONT PANEL LINE DRAWING

### Introduction

The T1/FT1/VF Drop & Insert Interface Module plugs into the IDS Bit Error Rate Test Set base units listed on the cover page and provides the base units with the ability to perform error rate and VF testing on full T1 (framed or unframed) or Fractional T1 circuits. Selectable Line Build Out and receiver ALBO allow testing of long haul lines or DSX circuits.

This module allows one or more channels to be dropped and new data inserted while passing the rest of the receive channels unaltered. Thus testing of one or more individual channels can be performed without taking down the whole T1 link. An Active Channel Detect mode facilitates determination of active and idle channels which are displayed on 24 active channel LEDs.

VF modes enable PCM VF channels to be tested. An internal digital milliwatt and digital reference generator allows insertion of standard 0 dBm, 1 KHz or 1004 Hz test tones. VF robbed bit signalling is displayed on 4 LEDs and is controlled by switches. Two Bantam VF connectors are provided for connection of an external VF test set for more extensive testing.

VF channel audio can be monitored with a small built-in speaker with volume control.

LEDs are used to display channel binary data and to indicate alarms. Slide and DIP switches are used to configure the module. A T1 circuit can be passively monitored by not connecting the module's transmitter.

### Fractional T1 Data Testing

Both contiguous and non-contiguous Fractional T1 Data may be tested in either a T1 circuit termination or Drop & Insert mode. DS0 channel rates of 56K and 64K may be selected. The test patterns are generated and tested by the base unit. In the non Drop & Insert configuration, DS0 channels not used for the Fractional T1 data will contain an idle code. In Drop & Insert configuration, DS0 channels not selected as data will be passed through unaltered from the receiver. Pattern testing on a single DS0 or any combination of multiple DS0s can be performed by selecting the desired channel(s) with the channel select DIP switches.

### VF Testing

Any one of the 24 DS0 channels may be selected and tested in either a T1 circuit termination or Drop & Insert mode. Robbed bit signalling is displayed for the receive side and switches allow control of the signalling for transmit. Four signal bits (A, B, C, and D) are controlled and displayed for ESF framing. Two bits (A and B) can be set to a 1, 0, or TOGGLE (alternating between 0 and 1) for D4 and SLC-96 framing. Robbed bit signalling may be disabled for systems using out of band signalling such as ISDN.

A Mu-Law CODEC is used to perform VF PCM encoding and decoding. A VF connector allows an external VF test set (such as the IDS Model 96 Analog Test Set or Model 970 TIMS) to be used to perform much more extensive VF tests.

A speaker with volume control enables the user to listen to the selected channel. Eight LEDs display the channel PCM contents in binary. An idle code or digital milliwatt can also be inserted into the selected channel. A switch on the back of the module allows selection of the standard 1000 Hz digital milliwatt or a 1004 Hz digital reference signal.

In non Drop & Insert configuration, the channels not being tested will contain a 7F hex idle code. In Drop & Insert configuration, the channels not being tested are passed through unaltered from the receiver.

### Digital Milliwatt/Digital Reference Signal

The module contains a digital tone generator that can be used during the VF and VF DROP & INSERT Test Configurations when the VF Insert switch is set to DIG MW. A slide switch on the back of the module allows selection of the standard 1000 Hz, 0 dbm digital milliwatt or a 1004 Hz, 0 dbm digital reference signal. Both of these signals are based on AT&T TR 43801.

The digital milliwatt is a digital representation of a 1 Khz, 0 dbm, sine wave. It is an 8 byte repeating pattern that consists of the following hex codes: 1E, 0B, 0B, 1E, 9E, 8B, 8B, 9E. The digital milliwatt should only be used to align channel banks. It should not be used over the network because it can cause false framing in some network equipment.

The digital reference signal is the digital representation of a 1004 Hz, 0 dbm sine wave. The digital pattern repeats on 250 msec intervals and will not cause any framing problems in a network. It can also be used to align a channel bank.

When shipped by IDS, the switch is set to the 1004 Hz position. This should be used for most applications to prevent network framing problems.

## FRONT PANEL DESCRIPTION

### T1 Connectors

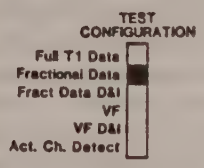
Two Bantam jacks at the top of the module, labeled T1 Rx IN and Tx OUT, provide the physical connection to the T1 circuit. Adapters are available for connection to DB-15, 310, and RJ45 jacks.

### VF Connectors

Two Bantam jacks at the bottom of the module, labeled EXT VF IN and OUT, allow connection to external VF equipment (such as the IDS Model 96 Analog Test Set or Model 970 TIMS) during VF testing. A standard Mu-Law CODEC (COder/DECoder) is used. The VF input and output impedance of the module is 600 ohms. Adapters are available for connection to 310 jacks.

## FRONT PANEL SWITCHES

### Test Configuration Switch



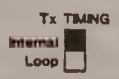

This six-position slide switch allows selection of the type of test to be performed. Selections are FULL T1 DATA, FRACTIONAL T1 DATA, FRACTIONAL T1 DATA DROP & INSERT, VF, VF DROP & INSERT, and ACTIVE CHANNEL DETECT. This switch determines which of the remaining switches are valid.

### Frame Format Switch

This four-position slide switch allows selection of the T1 frame format. Selections are D4 (Superframe Format), ESF (Extended Superframe Format), *SLC-96, and UNFRAMED. UNFRAMED is used to test the full 1.544 Mbps bandwidth and can be used on circuits that do not require any framing. UNFRAMED should not be used on a network that expects framing as network alarms will occur. The Test Configuration must be FULL T1 DATA and the DS0 Rate must be 64K for UNFRAMED testing. The D4 selection is also used for D1D, D2, and D3 channel banks which also use the Superframe Format. Refer to the appendix for the DS0 timeslot to channel mapping.

(*SLC is a registered trademark of AT&T)

### Tx Timing Switch




This two-position slide switch allows the transmit timing to be either the INTERNAL 1.544 MHz crystal oscillator or the clock recovered from the received data (LOOP). In systems slaved to a central timing source LOOP TIMING must be selected to prevent slips. For Drop & Insert tests, LOOP must be selected to allow the transmitter to be synchronized to the receiver. The LOOP selection causes a de-jittered clock based on the received data to be used as a timing source for transmit data. If the receive T1 signal is lost while LOOP timing is selected, an internal 1.544 MHz crystal oscillator is used for transmit timing until the receive signal is restored. The internal 1.544 MHz oscillator is accurate to 25 PPM and meets AT&T Stratum 4 requirements.

### DS0 Rate / VF Signalling Switch

This two-position slide switch performs a dual function. For data test configurations, it controls the DS0 rate. For VF test configurations, it is used to enable or disable the robbed bit signalling.

For Full T1 Data, Fractional T1 Data, and Fractional T1 Data Drop & Insert tests, this two position slide switch allows selection of 56K or 64K DS0 rates. The selection is based on network restrictions. When 64K is selected, all 8 bits of each channel contain pattern data, providing clear channel capability. When 56K is selected, only 7 bits of each channel contain data. The eighth bit is always a one to assure minimum ones density on the system or network. 64K must be selected when performing UNFRAMED testing.

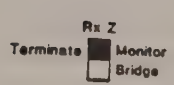
For VF tests, this switch is used to enable or disable robbed bit signalling. Robbed bit signalling is an in-band system that uses one bit position of the PCM code word every sixth frame for signalling. Applications such as ISDN that use out-of-band signalling on a separate "D" channel should have the module signalling turned off. The module inserts and extracts the signalling bits if signalling is enabled.

### Line Code Switch

This two-position switch determines the line code to be used by the module. The selection is dependent on network or system requirements. The B8ZS selection causes the module to use the Bipolar with 8 Zero Substitution method of zero suppression which provides clear channel capability. Sequences of 8 zeros are replaced with a code word containing intentional bipolar violations at defined points. Network equipment supporting B8ZS and the interface module receiver recognize this code word and restores the 8 zeros. These intentional bipolar violations are not counted as BPV errors.

The AMI selection provides standard Alternate Mark Inversion without zero suppression. This is used with network equipment that does not support B8ZS clear channel coding. The data source must assure the proper ones density. It should be noted that the ones density is always met with the 56K DS0 rate selection because the eighth bit of each channel is set to a one.

### Rx Impedance Switch

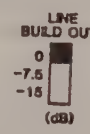



This two-position slide switch controls the input impedance of the receiver.

In the TERMINATE/MONITOR position, the receiver input impedance is 100 ohms. This position is used when the interface module will be terminating the link or connected to a resistor isolated monitor jack.

The BRIDGE position increases the receiver input impedance to 1 K ohms. This is used to passively bridge across a circuit that is already terminated and is not equipped with monitor jacks. The transmitter impedance is always 100 ohms.

### Line Build Out Switch

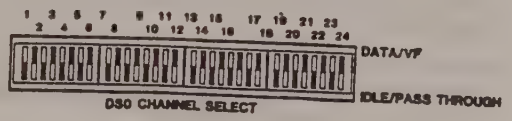



This three-position slide switch allows the selection of three levels of line build out. 0 dB is used when connecting at the DSX point or to simulate the signal at the output of a short cable. The -7.5 dB and -15 dB selections simulate the signal level and distortion at the output of longer cables having a loss of 7.5 dB and 15 dB respectively for long haul applications.

### VF Insert Switch

This three-position slide switch selects the data to transmit in the selected channel during VF tests. The selections are IDLE, DIGITAL MW, and EXT VF. The IDLE selection transmits an idle code word (7F Hex). The DIGITAL MW transmits the standard digital milliwatt or a digital reference signal. A switch on the back of the module selects which signal is used. The EXT VF selection transmits a PCM digital representation of the VF input on the VF input jack. A standard Mu-Law encoder is used in the module. This switch has no effect for the FULL T1 DATA, FRACTIONAL T1 DATA, FRACTIONAL T1 DATA DROP & INSERT, and ACTIVE CHANNEL DETECT test configurations.

### DS0 Channel Select Switches




Twenty-four two-position dip switches are used to select the DS0 channels for the Fractional T1 Data and VF test configurations. One position is labeled Data/VF and the other Idle/Pass-through.

For Fractional T1 data tests, one or more switches in any combination may be switched to Data/VF. These channels will contain the test pattern data. The remaining channels will be idle (7F Hex for non Drop & Insert configuration) or contain unaltered passed through receive data (for Drop & Insert configuration).

For VF test configurations, only one channel can be selected at a time. A setup error will occur if more than one channel is selected. The selected channel will contain the VF (based on the VF insert switch) and signalling (based on the signalling switches if enabled) data. The remaining channels will be idle (7F Hex for non Drop & Insert configuration) or contain unaltered passed through receive data (for Drop & Insert configuration). Refer to the appendix for the VF channel and timeslot number assignments.

These switches have no effect in the Full T1 test configuration which always uses all 24 channels, or the Active Channel Detect test configuration.

### Tx Signalling Switches

Four dip switches are used to control the transmit robbed bit signalling for the VF test configurations. Signalling must be enabled (with The VF/DS0 Rate Switch) in order to control the signalling bits. The switches are labeled A, B, C, and D. Each switch can be set to 1 or 0. These control the robbed bit signalling that is transmitted in the selected channel. These switches have no effect in the FULL T1 DATA, FRACTIONAL T1 DATA, FRACTIONAL T1 DATA DROP & INSERT, and ACTIVE CHANNEL DETECT test configurations. These switches also have no effect if the VF/DS0 Rate switch is set to NO SIG.

### D4 and SLC-96 Tx Signalling

D4 and SLC-96 framing formats use two signal bits, A and B. The module allows each of these two signal bits to be set to one of three states: 1, 0, or alternating 1/0. Two DIP switches control each signal bit. Switches A and C control the A signalling bit and switches B and D control the B signalling bit. If both switches are set to 1, the signal will be a 1. If both switches are set to 0, the signal will be a 0. If one switch is 1 and the other 0, the signal will alternate between 0 and 1 on each superframe.

### ESF TX Signalling

The ESF frame format uses four signal bits, A, B, C, and D. The module allows each of these four signal bits to be set to a 1 or 0. These are directly controlled by DIP switches A, B, C, and D.

## INDICATOR LEDS

### Rx Signalling LEDS

These four green LEDs display the status of the robbed bit signalling bits for receive side of the selected channel during VF test configurations if signalling is enabled (with the VF/DS0 Rate switch). They are labeled A, B, C, and D. LEDs A and B are used for D4 and SLC-96 frame formats. All four LEDs are used for the ESF frame format.

The LED is lit when the corresponding signal bit is a one. The LED is off when the corresponding signal bit is a zero. If the signal bit is alternating 1/0, the LED will be slightly dimmer than if the signal is a 1. These LEDs are off during FULL T1 DATA, FRACTIONAL T1 DATA, FRACTIONAL T1 DATA DROP & INSERT, and ACTIVE CHANNEL DETECT test configurations. These LEDs are also OFF if the VF/DS0 Rate switch is set to NO SIG.

### Data LEDS

These eight green LEDs display the binary channel contents for the receive side of the selected channel during VF test configurations and Fractional test configurations when only one DS0 channel is selected. They are labeled 1 to 8 and are lit when the bit is a one and off when the bit is a zero. Bit 1 is the PCM sign bit, which is the first bit sent. Bit 8 is the least significant PCM bit and is the bit position used for robbed bit signalling. These LEDs are off during FULL T1 DATA and ACTIVE CHANNEL DETECT test configurations. These LEDs are also off during FRACTIONAL T1 test configuration when more than one DS0 is selected.

### Active Channels LEDS

Twenty-four green LEDs are provided to inform the user as to which channels are being used for a test. All 24 LEDs are turned on for the FULL T1 DATA test configuration.

For the FRACTIONAL T1 DATA and VF test configurations, the LEDs indicate the channel or channels selected by the Channel Select DIP switches. The remaining channels contain the idle code.

For the FRACTIONAL T1 DATA DROP & INSERT and VF DROP & INSERT test configurations, the LEDs indicate the channels that are being dropped and inserted. The remaining channels are passed through from the receiver.

For the ACTIVE CHANNEL DETECT test configuration, the receiver examines each channel. The LEDs are turned on for channels that are not idle. Channels that contain a fixed 8-bit pattern having at least 2 one bits are determined to be idle.

### Setup Error LED

This red LED is used to warn of invalid switch settings. It blinks when the module switch settings are invalid for the selected test configuration. An AIS (Blue Alarm) is generated by the module transmitter when the setup is invalid. The invalid switch combinations are listed below:

– More than one channel selected for VF tests.

– TX TIMING set to INTERNAL for DROP & INSERT tests.

– FRAME FORMAT is UNFRAMED when the TEST CONFIGURATION is not FULL T1 DATA.

– DS0 RATE is set to 56K when the FRAME FORMAT is UNFRAMED.

Note that the Setup Error LED does not indicate if the switch settings are proper for the particular T1 connection under test. It only indicates if the switch settings are valid for the particular Test Configuration selected. Incorrect switch settings can corrupt or disable the circuit during Drop & Insert tests.

### Frame Sync LED

This green LED provides a real time indication that the interface module receiver has locked onto the incoming T1 signal framing pattern. The module checks the incoming data stream for frame synchronization by searching for the framing pattern based on the frame format switch.

For the D4 and SLC-96 Frame Formats, the interface module receiver searches for both the $F_t$ and $F_s$ patterns to synchronize. For the ESF Frame Format, the module receiver searches for the FPS pattern and verifies it with the CRC6 to synchronize. When the pattern is verified, the module receiver is in FRAME SYNC and the LED lights. The framing pattern is then continuously monitored for frame bit errors. The FRAME SYNC LED is turned off when 2 out the last 5 framing bits are in error.

The following framing bits are checked for errors: $F_t$ and $F_s$ for D4, $F_t$ for SLC-96, and FPS for ESF Frame Formats. The interface module receiver is in an Out Of Frame (OOF) condition when this LED is off. An extended OOF will generate a RED or BLUE ALARM. The FRAME SYNC LED does not light when the Frame Format is UNFRAMED.

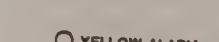
### Red Alarm LED

This red LED indicates an extended loss of local frame sync (Out Of Frame) or signal (Loss Of Signal) for any format except UNFRAMED. OOF is defined by the module as 2 out of the last 5 framing bits in error. Refer to the description of the FRAME SYNC LED for more details. The RED ALARM LED lights after 2.5 seconds of continuous OOF or LOS condition in the receiver.

For an intermittent OOF or LOS condition, an integration process that decays at 1/5 of the rise rate is used to count the 2.5 seconds. (For a 1/5 rate 100 msec OOF would require 500 msec of frame sync for the integration counter to reach 0.) The LED turns off when no OOF or LOS condition exists for two seconds. Note that if the module is OOF due to the reception of a BLUE ALARM, a RED ALARM will not be declared. While the RED ALARM is active the base unit will display the following message:

RED ALARM
LOST LOCAL FRAME SYNC

### Yellow Alarm LED




A YELLOW ALARM is a specific, frame-type dependent bit pattern which is transmitted by downstream network equipment in response to their receiver losing frame synchronization (RED ALARM detection).

In the D4 and SLC-96 framing formats, a yellow alarm is declared if bit 2 of all channels is a 0 for at least 254 occurrences in 256 consecutive channels. In the ESF format, a yellow alarm is declared if a repeating pattern of 00FFH is detected in the FDL for fifteen out of a possible sixteen repetitions. The module continuously monitors the incoming data stream for a YELLOW ALARM signal when a framed Frame Format is selected. If the YELLOW ALARM pattern is detected, the yellow YELLOW ALARM LED is turned ON and the base unit will display the following message:

YELLOW ALARM
LOST REMOTE FRAME SYNC

### Blue Alarm LED

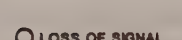
The module continuously monitors the incoming data stream for an AIS (Alarm Indication Signal). A BLUE ALARM is declared whenever the module receiver is OOF and an unframed all ones pattern (less than 5 zeros are detected in a three msec window) is received when a framed Frame Format is selected. Upon detection, the red BLUE ALARM LED is turned ON. The module AIS detection is error tolerant, so a BLUE ALARM will be detected with the presence of a bit error rate of $10^{-3}$.

A BLUE ALARM indicates that a transmission fault or other action has occurred upstream which has caused a signal disruption. An upstream device in loopback mode

can also send the AIS. The upstream device is sending the AIS signal in order to maintain network timing integrity.

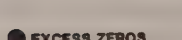
Note that a BLUE ALARM has priority over a RED ALARM, so even though the module receiver is OOF during a BLUE ALARM, a RED ALARM is not declared. No message is displayed on the base unit for a BLUE ALARM.

### Loss Of Signal LED



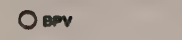

The module continuously monitors the receive signal for bipolar data activity. If the receiver detects 192 consecutive zeros, the yellow LOSS OF SIGNAL LED is turned ON. The base unit will display the message **LOSS OF CARRIER** or **LOSS OF SIGNAL.** Note that this message has priority over other messages, so even if the RED ALARM LED is ON (which will occur with an extended loss of signal), the LOSS OF CARRIER/SIGNAL message is displayed. If the signal is lost while the TX Timing is set to LOOP, a 1.544 MHz crystal controlled clock source will be used for the TX timing.

### Excess Zeros LED




The interface module receiver continuously monitors the raw incoming data stream (before the B8ZS decoder) for an excessive number of consecutive zeros. The number of zeros considered excessive is dependent by the Line Code selection. When the Line Code is B8ZS, any 8 consecutive zeros, including framing bits, will cause the yellow EXCESS ZEROS LED to light for a minimum of 2 seconds. A properly functioning B8ZS coded system will replace any occurrence of 8 zeros with the B8ZS code word which contains ones. When the Line Code is AMI, 16 consecutive zeros, including framing bits, are required to cause an EXCESS ZEROS alarm indication. AMI coded equipment should not send more than 15 consecutive zeros.

### BPV LED




The module continuously monitors the incoming data stream for unintentional Bipolar Violations. Unintentional BPVs are any BPV that are not part of a B8ZS code word.

The yellow BPV LED will light within one second for a minimum of 2 seconds whenever an unintentional BPV occurs.

The base unit also counts unintentional BPVs in the DSX ERR or BIPOLAR mode. Refer to next section.

## OPERATION

### DSX/Bipolar Error Counters

The base unit counts Framing errors, CRC-6 errors, and unintentional Bipolar Violations in the DSX ERR Mode (Model 76B) or BIPOLAR Mode (Model 77). The interface module issues a pulse to the base unit each time one of these errors occur.

The interface module has internal counters for unintentional BPVs (those that are not part of a B8ZS code word), CRC-6 errors, and Frame errors. These errors are counted for one second intervals and then transferred to registers. The counters are cleared immediately after each transfer. The module then synthesizes a series of pulses based on the register count so the base unit can count the various errors. This results in an average delay of 1/2 second and a maximum delay of one second before an error pulse is passed to the base unit.

If the T1 error rates are extremely high, it is possible to miss some of the errors if the interface module counter saturates during a one second count interval. If the number of errors exceed the saturation point, additional errors will not be counted during the one second interval. The saturation point is 65,535 for Bipolar Violations and 255 for Frame Errors.

All CRC-6 errors in the ESF Frame Format are always counted as the counter is large enough to count all CRC-6 errors that occur in a one second interval.

### Frame/CRC Error LED

The module continuously monitors the incoming data stream for frame bit errors ($F_t$ and $F_s$ for D4, $F_t$ for SLC-96, and FPS for ESF Frame Formats) and CRC-6 errors (for the ESF Frame Format). If an error is detected, the yellow FRAME/CRC ERROR LED is lit within one second for a minimum of 2 seconds. No frame bits are checked when the Frame Format is UNFRAMED. The base unit also counts CRC-6 and Frame errors in the DSX ERR or BIPOLAR mode.

### Speaker

A small speaker is used to monitor the channel in the VF Test Modes. The PCM channel data is converted to audio using a Mu-Law decoder. An amplifier is used to increase the power to drive the internal speaker. The speaker may be disabled by turning the volume all the way down. An external VF test set can be used to provide louder audio with better fidelity. The speaker is not used during the FULL T1 DATA, FRACTIONAL T1 DATA, FRACTIONAL T1 DATA DROP & INSERT, and ACTIVE CHANNEL DETECT Test Configurations.

### Volume Control

This control is used to control the volume of the speaker during the VF Test Configurations. If the volume is turned too high, the speaker may be over-driven resulting in distortion. The speaker may be disabled by turning the volume all the way down.

## POWER UP SELF-TEST

At power up, the module performs an internal self-test. The LEDs are all lit for approximately 4 seconds. During this time, the program storage EPROM and some of the hardware are tested.

If an error is detected, the ALARM and SETUP ERROR LEDs will blink an error code and normal operation of the interface module is not possible. If no errors are detected, the module is set up according to the various switches.

### Power Up Self-Test Error Codes

Power Up self-test errors are identified by blinking error codes on the Setup Error and Alarm LEDs. Any error code is displayed after lamptest and is repeated continuously.

| # BLINKS | TEST FAILURE |
|---|---|
| None | All tests passed |
| 1 | EPROM Checksum Error |
| 2 | Switch Error - Test Configuration switch |
| 3 | Switch Error - Line Build Out switch |
| 4 | Switch Error - VF Insert switch |
| 5 | T1 Framer Chip Error |
| 6 | No Interrupt from T1 Framer Chip |
| 7 | Counter Chip Error |

## SETUP

The module is set up by using the front panel slide and DIP switches. The proper module switch settings must be made in order to match the parameters of the T1 network under test. The SETUP ERROR LED will blink if an invalid combination of switches for a particular test configuration is used. The SETUP ERROR LED does not indicate if a particular switch configuration is incorrect for the T1 link being tested. An incorrect configuration during drop and insert testing can disrupt the T1 link.

Refer to the following sections for descriptions of the valid switch settings for each of the Test Configurations. Whenever certain setup switches are changed, the module is reset (which results in a receiver re-frame operation.) These switches are the ones that cause a major setup change and include: TEST CONFIGURATION, FRAME FORMAT, TX TIMING, LINE CODE, and DS0 RATE/SIGNAL.

The base unit should also be reset any time one of these switches are changed in order to avoid the display of erroneous data. During drop and insert testing, these switch changes should be kept to a minimum to avoid disruptions to the passed through data stream.

### Full T1 Data Configuration

The FULL T1 DATA Test Configuration allows testing of a T1 circuit which utilizes the full bandwidth (Framed or Unframed) available for data transmission.

### Unframed

When the Frame Format is set to UNFRAMED, the full 1.544 Mbps is used for pattern transmission and no framing pattern is sent or expected for the receiver. The DS0 rate must be 64K when UNFRAMED is selected. UNFRAMED should not be used on circuits that expect framing because of the alarms that will be generated.

### Framed

For the framed formats, all 24 channels are used at either a 56K or 64K DS0 rate. For 64K DS0 channels, 1.536 Mbps are used for pattern transmission and 8 Kbps are used for framing. For 56K DS0 channels, 1.344 Mbps are used for the pattern, 8 Kbps for framing, and 192 Kbps are used for the "ones" forced into the eighth bit of each channel.

The user must select the proper Frame Format, Tx Timing source, DS0 rate, Line Code, Line Build Out, and Receiver Termination. The Channel Select and VF switches are ignored. All of the Active Channel LEDs are lit to indicate that all 24 DS0 channels are used. The base unit can perform Bit Error Rate, Block Error Rate, or an Error Free Seconds test using either pseudo-random or fixed patterns. Alarm conditions are reported by LEDs on the module. Loss of Carrier/Signal, Red Alarm, and Yellow Alarm messages are also displayed on the base unit LCD display. The overall T1 frame is analyzed by the interface module for alarm conditions and T1 associated errors.

### SLC-96* Message Format

(*SLC is a registered trademark of AT&T)

SLC-96 uses the D4 $F_s$ bits to perform the dual function of signal framing and data link. Twelve bits of the D4 $F_s$ framing pattern are sent followed by 24 bits for the data link in the $F_s$ bit positions for a total of 36 bits sent over a six superframe interval. The Ft framing pattern is sent normally. The data link consists of four message fields with interspersed spoiler bits. The spoiler bits prevent false framing in cases where a message field resembles a framing pattern. The module transmitter sends the following mes-

sages repetitively when not operating in a Drop & Insert test configuration:

Concentrator Field (12 bits): MESS4 (11111110000B) This is an idle code.

Maintenance Field (3 bits): 111B This is the code for no maintenance message.

Alarm Field (2 bits): 11B This is the alarm field framing message. No alarm messages are sent.

Line Switch Field (4 bits): 1111B This is the idle state.

These codes are based on Bellcore Technical Reference TR-TSY-000008 Issue 2, August 1987.

When operating in a Drop & Insert Test Configuration, the received SLC-96 data link is passed to the interface module transmitter unaltered.

### ESF FDL Contents

When operating in the FULL T1, FRACTIONAL T1 DATA, or VF Test Configurations with the Frame Format set to ESF, the interface module generates the ESF Facility Data Link data. The interface module sends continuous flags (7E Hex) to make the FDL appear idle.

When operating in a Drop & Insert Test Configuration with an ESF Frame Format, the received FDL is passed to the interface module transmitter unaltered.

### Fractional T1 Data Configuration

The FRACTIONAL T1 DATA Test Configuration uses the same setup configuration as FULL T1 except that the Channel Select switches are active and the Frame Format must not be UNFRAMED. With Fractional T1, the bandwidth available is determined by the number of 56K or 64K channels leased. The channels not containing data must contain an idle code. If a user has leased a one quarter T1 and uses 64K channels, 6 channels would be available and the effective data rate would be 384 Kbps (64K * 6). If the channel rate is 56K, the effective data rate would be 336 Kbps (56K * 6). Data channels may be either contiguous or non-contiguous.

### Contiguous Channels

Contiguous channels are a group of consecutive channels utilized for data transmission, such as channels 1, 2, 3, 4, 5, and 6. This channelization requires the user to adhere to minimum pulse density requirements. This can be achieved by using either 56K channel rates which forces bit 8 in each channel to a one, or by using 64K channels with B8ZS.

### Non-contiguous Channels

Non-contiguous channels are alternate channels in a frame, such as channels 1, 3, 5, 7, 9, and 11. This is required when operating with an AMI Line Code and 64K channels. The idle code word in the alternate unused channels insures minimum pulse density. In non contiguous Fractional T1, the data in each channel may encounter different delays due to different routing through the network. If this occurs, the base unit will not sync up with a pseudo-random pattern selected. However, it will sync up with a MARK when the DS0 rate is 56K or a MARK, ALTERNATE, or 1 IN 8 pattern when the DS0 Rate is 64K. This is because these patterns are repetitive on a channel basis and will not be affected by different delays. In order to perform pseudo-random testing in this case, the user will have to run the test in each channel individually.

### 24 Channel Select Dip Switches

The 24 Channel Select DIP switches allows selection of which channels contain DATA and which will be IDLE. Any combination of DATA and IDLE channels is allowed by the interface module. The channels selected as DATA will be analyzed by the base unit receiver for pattern checking. The transmit pattern from the base unit will is sent serially in the selected DATA channels and an idle code word (7F Hex) is sent in the channels selected as IDLE. Refer to Full T1 Data Configuration for the Data Link Message contents for SLC-96 and ESF Frame Formats.

### Fractional T1 Data Drop & Insert Configuration

The FRACTIONAL T1 DATA DROP & INSERT Test Configuration uses the same setup configuration as FRACTIONAL T1 except that the Channel Select switches now control which channels contain DATA Dropped to/Inserted from the base unit and which channels are passed through unaltered. The TX Timing must be set to LOOP to allow the transmitter to be synchronized to the receiver. The receive data and clock is passed through a de-jitter circuit to provide a stable transmit clock. Drop & Insert operation allows tests to be performed on one or more channels without altering the rest of the channels. The framing bits are regenerated by the transmitter. Any framing bit errors detected by the receiver are not passed through. The SLC-96 or ESF data link is passed through from the receiver unaltered. The ESF CRC-6 is re-computed in the transmitter.

When connecting to the network equipment under test, the interface module RX IN should be connected in a bridge mode or to a monitor jack first. This allows the module receiver to frame up on the T1 data stream. Verify proper framing and operation by the FRAME SYNC, ALARM and T1 ERROR LEDs. The FRAME SYNC LED should be continuously lit and no alarm or T1 error LEDs should be lit. If all appears well, the module TX OUT may be connected. A momentary "hit" will occur downstream when the transmitter is first plugged in because of a change of frame alignment due to the T1 signal delay added by the interface module.

The interface module receiver will drop the channel or channels selected to be DATA to the base unit for pattern checking. The rest of the receive channels will be passed unaltered to the module transmitter. The transmitter will insert pattern data from the base unit into the same channels set to DATA. The channels set to PASS THROUGH are unaltered (except for some delay through the module receiver, de-jitter logic, and transmitter).

If the receive signal is lost, the module transmitter will send an unframed all ones pattern downstream using an internal 1.544 Mhz clock. This AIS or "Blue Alarm" signal is used to maintain transmission continuity and to notify downstream equipment of the fault.

When disconnecting the interface module from the network, the module transmitter should be disconnected first. A momentary hit (Change Of Frame Alignment) will occur downstream due to the T1 signal delay of the module being removed from the circuit. The module receiver may now be disconnected.

### VF Configuration

The VF Test Configuration allows testing of any of the 24 VF channels on a T1 circuit. All switches need to be set up. The base unit does not perform any pattern tests for VF modes. DSX ERR or BIPOLAR Mode may be selected on the base unit to count BPV, Framing, and CRC-6 errors during VF tests. Only one of the 24 Channel Select switches may be set to VF at a time. The channel that is set to VF will be connected to the VF circuits in the interface module. All other channels will have an idle code (7F Hex) on the transmit side and be ignored on the receive side. Refer to Full T1 Data Configuration for the Data Link Message contents for SLC-96 and ESF Frame Formats.

The overall T1 frame is analyzed by the interface module for alarm conditions and T1 associated errors. These are displayed on the LEDs and by the base unit LCD.

### VF Insert Switch

The VF Insert switch controls what is transmitted in the selected VF channel. The VF Insert switch allows selection of an IDLE code (7F Hex), DIGITAL MW (1 KHz digital milliwatt or 1004 Hz digital reference signal based on back panel switch - see page 2), or EXT VF (external signal input on the VF IN jack that is encoded with a Mu-Law coder).

### Signalling Switches

The Signalling switches control the robbed bit signalling that is sent if signalling is enabled. The selected VF channel is also dropped from the receive T1 signal. The binary channel data is displayed on the 8 data LEDs. The robbed bit signalling is displayed (if enabled) on the A and B LEDs for D4 and SLC-96 Frame Formats. The signalling is displayed (if enabled) on the A, B, C, and D LEDs for the ESF Frame Format.

### Audio

The audio (decoded by a Mu-Law decoder) for the selected channel is passed to the VF jack as well as through an amplifier for the speaker. The Volume Control is used to control the speaker volume.

### VF Jacks

The VF jacks allow an external VF test set to be used for more sophisticated tests such as variable frequency and level tone generation/measurement. The send and receive audio are both available in a 600 ohm line format. Test sets such as the IDS Model 96 Analog Test Set or Model 970 TIMS can be used.

### VF Drop & Insert Configuration

The VF DROP & INSERT Test Configuration uses the same setup configuration as VF except that the Channel Select switches now control which channel is Dropped to/Inserted from the module VF circuits and which channels are passed through unaltered. The base unit does not perform any pattern testing for VF modes. The TX Timing must be set to LOOP to allow the transmitter to be synchronized to the receiver. The receive data and clock is passed through a de-jitter circuit to provide a stable transmit clock. Drop & Insert operation allows VF tests to be performed on a channel without altering the rest of the channels. The framing bits are regenerated by the transmitter. Any framing bit errors detected by the receiver are not passed through. The SLC-96 or ESF data link is passed through unaltered. The ESF CRC-6 is recomputed in the transmitter.

When connecting to the network equipment under test, the interface module RX IN should be connected in a bridge mode or to a monitor jack first. This allows the module receiver to frame up on the T1 data stream. Verify proper framing and operation by the FRAME SYNC, ALARM and T1 ERROR LEDs. The FRAME SYNC LED should be continuously lit and no alarm or T1 error LEDs should be lit. If all appears well, the module TX OUT may be connected. A momentary hit will occur downstream when the transmitter is first plugged in because of a change of frame alignment due to the added T1 signal delay through the interface module.

The interface module receiver will drop the channel selected to be VF to the interface module VF circuits. The rest of the channels will be passed to the module transmitter. The transmitter will insert the selected VF (based on the VF Insert switch) and signalling (if enabled) into the channel set to VF. The channels set to PASS THROUGH

are unaltered (except for some delay through the module receiver, de-jitter logic, and transmitter).

If the receive signal is lost, the module transmitter will send an unframed all ones pattern downstream using an internal 1.544 Mhz clock. This AIS or "Blue Alarm" signal is used to maintain transmission continuity and to notify downstream equipment of the fault.

When disconnecting the interface module from the network, the module transmitter should be disconnected first. A momentary hit (Change Of Frame Alignment) will occur downstream due to the T1 signal delay of the module being removed. The module receiver may now be disconnected.

### Active Channel Detect

The ACTIVE CHANNEL DETECT Test Configuration selection provides the user the ability to determine which channels of a T1 link are being utilized for data or VF and which channels are idle. The same switch setup as FULL T1 DATA is used, except that the Frame Format must not be UNFRAMED.

The receiver sequentially monitors each channel of the framed T1 data stream. Channels that do not contain an idle pattern (a repeated 8-bit word with at least 2 one bits) will light the respective Active Channel LED. Channels that contain an idle pattern will have its respective LED off. The module transmitter continuously transmits idle characters (7F Hex) in each DS0 channel. If the transmitter is looped back to the receiver in this mode, all Active Channel LEDs will be off.

### Loop Up/Down

In order to perform a LOOP UP or LOOP DOWN via the base unit, the user must place the interface module into the FULL T1 configuration with 64K DS0 rate prior to initiating the LOOP UP/DOWN. Once the loop has been completed, the Test Configuration may be changed for testing Fractional or VF circuits. Refer to the base unit manual for details on performing Loop Up/Down.

### Stress Patterns

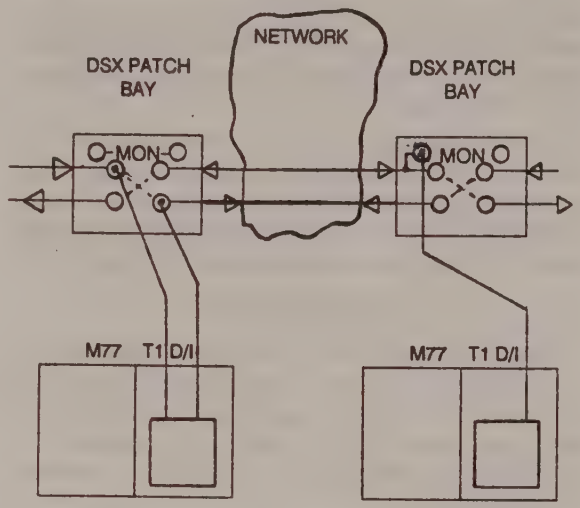
Stress patterns are used to stress a network by placing the maximum number of allowable zeros in the data field. The Models 76B and 77 have the 1 in 8 and 3 in 24 stress patterns. The Model 77 also has a user-defined pattern. In order to utilize the patterns effectively, they should only be used when the DS0 rate is 64K. With the 64K DS0 rate, the true channelized 1 in 8 or 3 in 24 test pattern is transmitted. The module transmitter will "Frame Lock" the base unit pattern generator to the T1 framing so that these patterns will not cause yellow alarms on D4 and SLC-96 circuits.

If the DS0 rate selection is 56K, then only 7 bits of the pattern will be placed in a channel because the eighth channel bit is forced to a one. The eighth bit of the stress pattern will be placed in the next data channel, thus shifting the pattern. The base unit will still achieve synchronization and not trigger alarms when operating with 56K DS0 channels, however, they will not stress the network as intended because it is already limited to a maximum of 7 zeros by the DS0 selection.

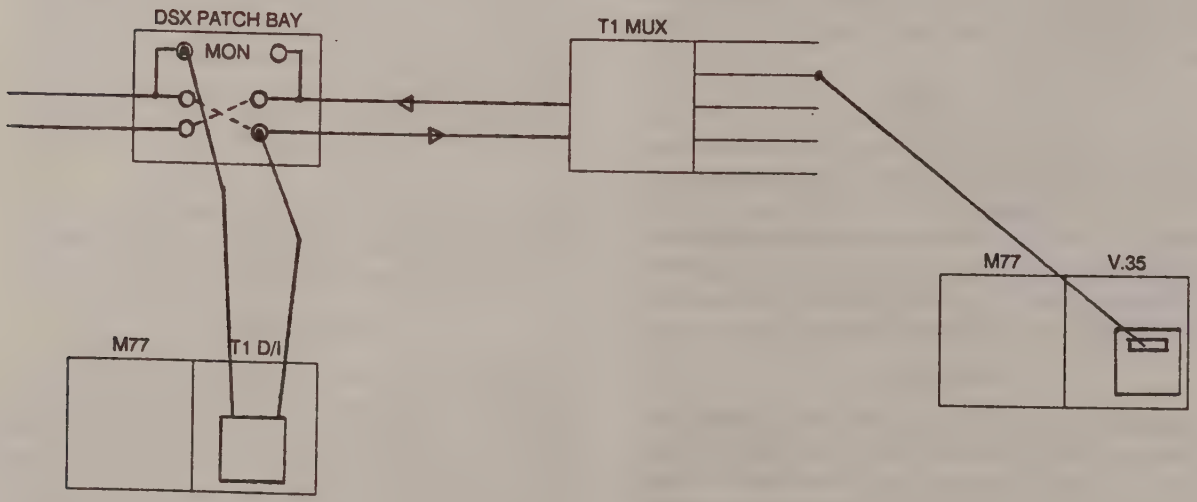
If the Test Configuration is FRACTIONAL DATA DROP AND INSERT and the module receiver encounters a change of frame alignment, the module will perform another "Frame Lock" operation to realign the base unit pattern generator to the new T1 framing. A change of frame alignment occurs when the module receiver loses receive frame synchronization and has a new frame alignment when frame sync is regained.

## TEST CHANNELS THROUGH A NETWORK

This connection allows testing of a channel or group of channels through a network. The test is run in a half duplex manner, with the first test set generating and inserting the test pattern into the selected channel(s) on the T1 link and the second test set dropping the channel(s) for error checking. The connections can be reversed to test in the other direction. The channels not being tested will still contain the user data.



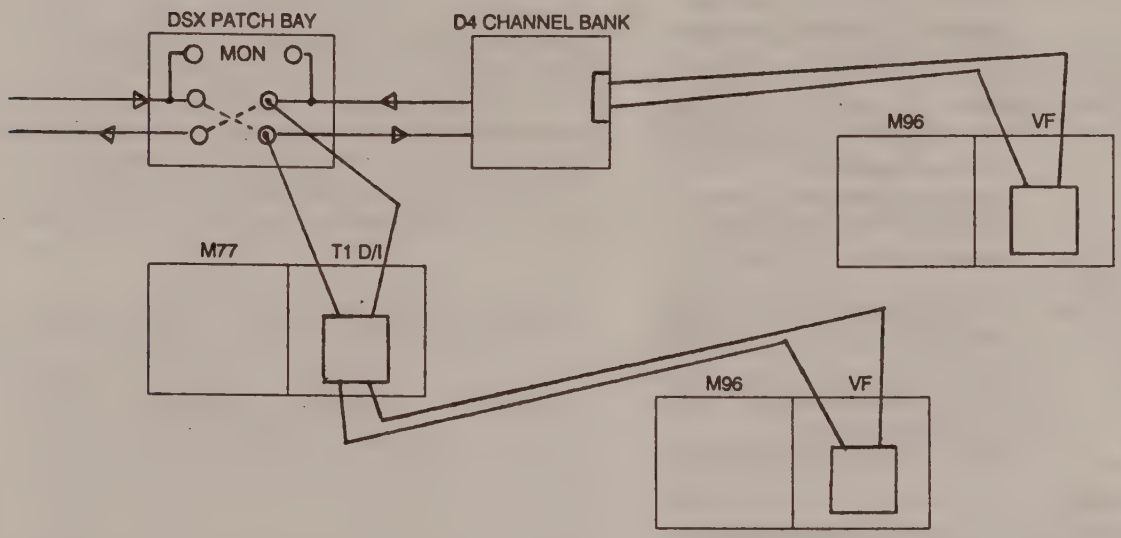

## TEST CHANNELS ON T1 MULTIPLEXER




This connection allows testing ports on a T1 multiplexer. The ports can be fractional T1 or a single channel. This example is a half duplex test with one Model 77 being used to insert the test pattern into the T1 data stream on the proper channel(s) and the second Model 77 receiving the pattern on a V.35 port. The remaining ports are still carrying user data.

To reverse the direction of testing, the Insert connection would be removed and the RX IN jack of the module would be connected to the other Monitor jack to allow dropping the pattern to the base unit.

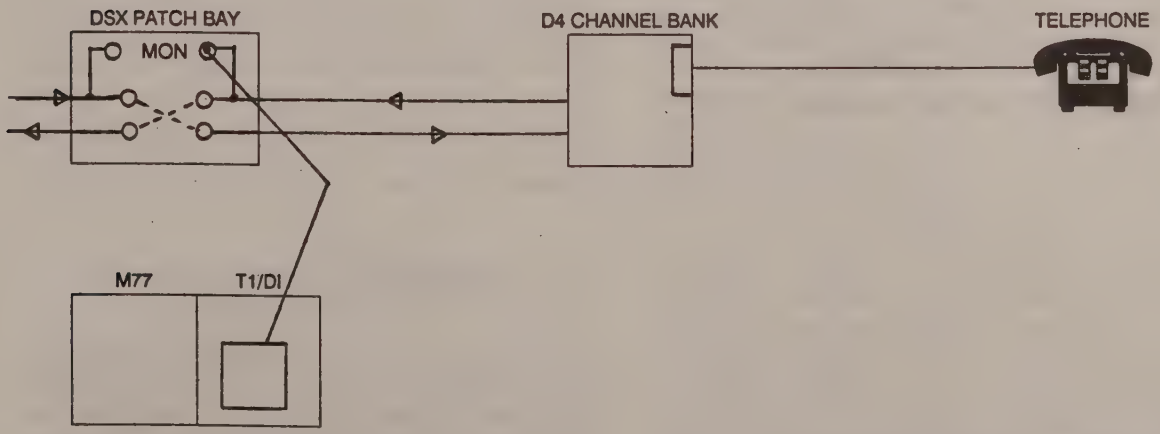
## TEST AND ALIGN CHANNEL BANKS




This connection allows a Channel Bank to be tested and aligned. The module is shown in a circuit terminate mode connection which disconnects the Channel Bank from the link. IDS Model 96 Voice Frequency test sets are used to perform full duplex VF tests of the selected channel. The Digital Milliwatt in the module can also be used. The CHANNEL SELECT switches are used to select the channel to be tested.

A Drop & Insert connection could also be used to perform a half duplex test on any selected channel without disrupting the remaining channels.

## MONITOR VF CHANNELS




This connection allows VF channels to be monitored. The channel signalling is displayed on the RX SIGNAL LEDs. The VF can be heard through the speaker and the PCM binary data is displayed on the DATA LEDs. Alarms are indicated by the LEDs. The base unit counts BPVs, Frame Errors, and CRC-6 Errors.

## SPECIFICATIONS

| | |
|---|---|
| Power | +5 Vdc 290 mA Max.<br>+9 to +12 Vdc 25 mAMax.<br>-10 to -12 Vdc 16 mAMax.<br>(provided by base unit via mating 37 pin "D" connector) |
| T1 Output | DSX-1 (0-133 feet); T1 CSU (0 dB, -7.5 dB, or -15 dB line build-out)<br>100 Ohm impedance<br>Jitter attenuation during Drop & Insert meets AT&T TR 62411 December 1990 |
| T1 Input | Automatic Line Build-out (ALBO)<br>Switchable 100 Ohm or > 1K Ohm impedance<br>Compatible with DSX-1 or long line<br>Jitter tolerance meets AT&T TR 62411 December 1990 |
| T1 Signal Delay during Drop & Insert | 25 to 153 bits (depending on jitter and wander of receive signal) |
| Internal T1 Clock Accuracy | 25 ppm, meets AT&T Stratum 4 requirements |
| VF Output | 600 Ohm impedance |
| VF Input | 600 Ohm impedance |
| Enclosure | Plastic Molded |
| Dimensions | 5.95" L x 5.60" W x 1.75" D |
| Weight | 1.5 lbs. |
| Temperature | Operating: 0°C to 50° C (+21° F to +122° F)<br>Storage: -20°C to +70° C (-4° F to +150° F) |
| Humidity | 90% maximum (non-condensing) |

# APPENDIX A
# VF CHANNEL AND TIMESLOT NUMBER ASSIGNMENT

## Introduction

The mapping of VF channels to T1 timeslots varies with the type of channel bank. The DS0 Channel Select switches on the T1/FT1/VF Interface Module select the T1/DS1 timeslot for testing. D3 and D4 type channel banks use a sequential mapping of channels to time slots so the switches directly represent the channels. D1D and D2 channel banks use different mapping which is listed in the table.

| DS1 Time Slots | D3/D4 Sequential Channel No.Assignment | D1D Channel Number Sequence Assignment | D2 Channel Number Sequence Assignment |
|---|---|---|---|
| 1 | 1 | 1 | 12 |
| 2 | 2 | 13 | 13 |
| 3 | 3 | 2 | 1 |
| 4 | 4 | 14 | 17 |
| 5 | 5 | 3 | 5 |
| 6 | 6 | 15 | 21 |
| 7 | 7 | 4 | 9 |
| 8 | 8 | 16 | 15 |
| 9 | 9 | 5 | 3 |
| 10 | 10 | 17 | 19 |
| 11 | 11 | 6 | 7 |
| 12 | 12 | 18 | 23 |
| 13 | 13 | 7 | 11 |
| 14 | 14 | 19 | 14 |
| 15 | 15 | 8 | 2 |
| 16 | 16 | 20 | 18 |
| 17 | 17 | 9 | 6 |
| 18 | 18 | 21 | 22 |
| 19 | 19 | 10 | 10 |
| 20 | 20 | 22 | 16 |
| 21 | 21 | 11 | 4 |
| 22 | 22 | 23 | 20 |
| 23 | 23 | 12 | 8 |
| 24 | 24 | 24 | 24 |

## SLC 96 CHANNEL AND TIMESLOT NUMBER ASSIGNMENT

The channel mapping for SLC 96 is dependent on the mode of operation. Modes I and III have a constant mapping that is listed in the tables. Mode II is concentrated resulting in a dynamic channel to time slot mapping. The Active Channel Detect test configuration can be used to determine active time slots on a SLC 96 Mode II system.

## SLC 96 Modes of Operation

The upper and lower shelf groups in an RT (Remote Terminal) can be independently operated in any one of three modes, but a shelf group's mode of operation restricts the numbers and/or types of channel units that may be located in it.

## SLC 96 Mode I

This refers to a nonconcentrated shelf group that is served by two Primary T1 lines. Each shelf in the shelf group is served by a dedicated T1 line given the same designation (A, B, C, or D) as the shelf. For example, if Shelf Group AB is operating in Mode I, its A Shelf will be served by the A T1 line and its B shelf by the B T1 line. If all twelve slots of a shelf are filled with dual-circuit channel units, the twenty-four time slots on the T1 line associated with that shelf will be fully used. Single-circuit channel units may be substituted for dual-circuit channel units without restrictions, but for each single-circuit channel unit that replaces a dual-circuit unit, one DS1 time slot on the T1 line will be unused.

| DS1 Frame Time Slot | Channel Number | | | |
|---|---|---|---|---|
| | Shelf A | Shelf B | Shelf C | Shelf D |
| 1 | 1 | 25 | 49 | 73 |
| 2 | 13 | 37 | 61 | 85 |
| 3 | 2 | 26 | 50 | 74 |
| 4 | 14 | 38 | 62 | 86 |
| 5 | 3 | 27 | 51 | 75 |
| 6 | 15 | 39 | 63 | 87 |
| 7 | 4 | 28 | 52 | 76 |
| 8 | 16 | 40 | 64 | 88 |
| 9 | 5 | 29 | 53 | 77 |
| 10 | 17 | 41 | 65 | 89 |
| 11 | 6 | 30 | 54 | 78 |
| 12 | 18 | 42 | 66 | 90 |
| 13 | 7 | 31 | 55 | 79 |
| 14 | 19 | 43 | 67 | 91 |
| 15 | 8 | 32 | 56 | 80 |
| 16 | 20 | 44 | 68 | 92 |
| 17 | 9 | 33 | 57 | 81 |
| 18 | 21 | 45 | 69 | 93 |
| 19 | 10 | 34 | 58 | 82 |
| 20 | 22 | 46 | 70 | 94 |
| 21 | 11 | 35 | 59 | 83 |
| 22 | 23 | 47 | 71 | 95 |
| 23 | 12 | 36 | 60 | 84 |
| 24 | 24 | 48 | 72 | 96 |

### SLC 96 Mode II

This refers to a shelf group that uses a concentrator and is connected to the LDS by one primary T1 line. The A T1 line is used for Shelf Group AB, and the C T1 line is used for Shelf Group CD. A maximum of 24 dual single party or multiparty channel units may be inserted into the channel unit slots in a Mode II shelf group which results in up to 48 lines competing for the twenty-four DS1 time slots and yields a 2:1 concentration ratio. Although either dual- or single-circuit channel units can be used in a Mode II shelf group, only the dual-circuit types are concentrated. The concentration ratio remains 2:1 even if single-circuit channel units are substituted for dual-circuit units since each single-circuit channel unit displaces a dual-circuit channel unit and permanently occupies one DS0 time slot.

In order to maintain sufficient traffic capacity, a minimum of 16 DS0 time slots on each T1 line must be available for concentrated traffic. Hence, a maximum of 8 single-circuit channel units may be present in a Mode II shelf group. Furthermore, in a SLC 96 RT, coin or D4 special service channel units may only be used in the four rightmost channel unit slots of each shelf. Data Link messages are used to assign channels to DS1 time slots.

### SLC 96 Mode III

This refers to a nonconcentrated shelf group that is served by one Primary T1 line. The A T1 line is used for Shelf Group AB, and the C T1 line is used for Shelf Group CD. This mode is used when a shelf group is equipped only with coin and D4 single-circuit channel units.

Channel Number/Time Slot Mapping
for SLC 96 Mode III

| DS1 Frame Time Slot | Channel Number | | | |
|---|---|---|---|---|
| | D4 Sequence | | D1D Sequence | |
| | Shelf Group AB | Shelf Group CD | Shelf Group AB | Shelf Group CD |
| 1 | 25 | 73 | 1 | 49 |
| 2 | 1 | 49 | 13 | 61 |
| 3 | 27 | 75 | 25 | 73 |
| 4 | 3 | 51 | 37 | 85 |
| 5 | 29 | 77 | 3 | 51 |
| 6 | 5 | 53 | 15 | 63 |
| 7 | 31 | 79 | 27 | 75 |
| 8 | 7 | 55 | 39 | 87 |
| 9 | 33 | 81 | 5 | 53 |
| 10 | 9 | 57 | 17 | 65 |
| 11 | 35 | 83 | 29 | 77 |
| 12 | 11 | 59 | 41 | 89 |
| 13 | 37 | 85 | 7 | 55 |
| 14 | 13 | 61 | 19 | 67 |
| 15 | 39 | 87 | 31 | 79 |
| 16 | 15 | 63 | 43 | 91 |
| 17 | 41 | 89 | 9 | 57 |
| 18 | 17 | 65 | 21 | 69 |
| 19 | 43 | 91 | 33 | 81 |
| 20 | 19 | 67 | 45 | 93 |
| 21 | 45 | 93 | 11 | 59 |
| 22 | 21 | 69 | 23 | 71 |
| 23 | 47 | 95 | 35 | 83 |
| 24 | 23 | 71 | 47 | 95 |

## APPENDIX B – FRAME SYNC LED APPLICATION NOTE

### Introduction

This application note explains the operation of the Frame Sync LED on the interface module with respect to the Frame Sync Locked and Lost LEDs on the base unit (Model 76B or Model 77). Under certain conditions it is possible for the interface module Frame Sync LED to be ON while the base unit Frame Sync Locked LED is OFF. The opposite condition can also occur.

### Interface Module Frame Sync LED

The Frame Sync LED on the interface module provides a real time indication of receiver frame sync. It is ON whenever the receiver has locked on the incoming framing pattern (D4, ESF, or SLC-96) and is OFF whenever 2 out of the last 5 framing bits are in error (OOF - Out Of Frame condition). The LED stays OFF when the UNFRAMED Frame Format is selected. The module receiver can be OOF and turn the Frame Sync LED OFF for any of the following reasons:

– UNFRAMED Frame Format is selected: The LED is normally OFF in this case because no framing is expected.

– Errors on the line: If too many frame bits (more than 2 out of the last 5) are in error, the receiver is OOF.

– Wrong Frame Format is selected: The receiver would be looking for a different framing pattern than is actually present.

– Loss of Signal: If the incoming signal is not present the module will be OOF. The Loss of Signal LED will also be ON.

– Blue Alarm: An AIS (Alarm Indication Signal) or Blue Alarm is an unframed all ones pattern. Since no framing bits are present, the receiver is OOF.

– Setup Error: If an invalid combination of switches is selected, the Setup Error LED will blink and the Frame Sync LED may be OFF.

### Interface Module Red Alarm LED

This LED lights to indicate an extended receiver OOF (that is not caused by an AIS or Blue Alarm) or Loss of Signal. The Red Alarm LED lights after 2.5 seconds of continuous OOF or LOS. The LED turns OFF when no OOF or LOS condition exists for 2 seconds. For an intermittent OOF or LOS, an integration process that decays at 1/5 the rise rate is used to count the 2.5 seconds. (For a 1/5 rate, 1 second of OOF or LOS would take 5 seconds of frame sync for the integration timer to reach zero.) While the Red Alarm LED is ON, the base unit displays: RED ALARM LOST LOCAL FRAME SYNC. This definition and timing of the Red Alarm is based on AT&T Technical Reference TR 62411.

### Base Unit Frame Sync Locked and Lost LEDs

The base unit indirectly determines Frame Sync status by monitoring the Interface Module's Red Alarm, Loss of Signal, and Unframed indications. If an Unframed Frame Format is selected, the LED remains off. If a Framed Frame Format (D4, ESF, or SLC-96) is selected, the base unit monitors the Red Alarm and Loss of Signal indications to determine Frame Sync. If no Red Alarm or Loss of Signal exists, the base unit Frame Sync Locked LED is turned ON. When either a Red Alarm or Loss of Signal occurs, the base unit turns the Frame Sync Locked LED OFF and the Frame Sync Lost LED ON. The Frame Sync Lost LED is turned OFF by the Reset/Resync button or a base unit configuration switch change. Note that the Model 76B indicates Frame Sync Locked and Lost only when the Mode is set to DSX ERR.

Because the Red Alarm is delayed from the actual OOF, the base unit Frame Sync Locked LED is delayed from the Module Frame Sync LED. For cases of intermittent OOF that are not severe enough to trigger a Red Alarm, the base unit Frame Sync Locked LED will remain lit. If the module Frame Sync LED is OFF due to an AIS (Blue Alarm), the base unit Frame Sync Locked LED remains lit.

For cases where a Loss of Signal occurs, the base unit Frame Sync Locked LED and the modules Frame Sync LED will closely track.

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### Features

- Supports Standard DDS and DDS with secondary channel
- Measures receive signal peak voltage and loss in dB
- Operates at 2.4K, 4.8K, 9.6K, 19.2K, 57K, and 64K
- Tests toward Network or user CSU/DSU
- Generates loop sealing current when testing CSU/DSU
- Responds to network CSU and DSU (non-latched or latched) loopbacks
- Generates CSU and DSU (non-latched or latched) loopbacks in CSU/DSU under test
- Auto Setup function to automatically determine setup parameters
- Supports extended receive range
- Tests point-to-point or multi-point circuits
- Tests primary or secondary channel
- Alarm and status LEDs with history
- Eight data LEDs display Rx data
- Dual RJ-48 jacks to connect to network or CSU/DSU
- Internal or Loop Tx timing
- Terminate or Bridge Rx impedance
- Indicates and counts BPV and Frame errors

### Introduction

The DDS Local Loop Interface Module plugs into the IDS Model 77 Bit Error Rate Test Set and provides the base unit with the ability to perform error rate testing on Digital Data System 4 wire local loop (customer loop) circuits and DDS customer premise CSU/DSU equipment. The module does not test inside the network at the DS0 or DS1 timeslot level. The module supports standard DDS and DDS with secondary channel (sometimes referred to as DDS-II). A 64K rate is also supported although this is not truly DDS. AT&T offers a 64K service that uses the DDS 72K loop structure in their ACCUNET Spectrum of Digital Services. Testing may be performed on either the primary or secondary channel. Point to point or multipoint circuits and equipment may be tested. The module responds to and can generate CSU, DSU non-latched, and DSU latched loopback commands. Color coded LEDs and displays indicate switch settings, Rx signal level, Rx data, activity, errors, and CSU/DSU loopback status.

### Network Testing

The DDS Local Loop Interface Module can operate as a CSU/DSU to perform tests toward the network. The module receiver performs automatic filtering and equalization for various line lengths. The receiver has extended range to operate with line losses that exceed the DDS specified 34 dB. The Rx level meter indicates the receive signal peak voltage or loss in dB with respect to a nominal, no loss, signal. An Extended Range LED lights to indicate when the receive level is lower than DDS specifications and will only operate with extended receive range equipment. The module will respond to CSU (Channel), DSU Non-Latching, and DSU Latching loopbacks. The module can also be forced into a loopback to loop data received from the network back to the transmitter. LED's indicate loopback status. The module tests for the presence of a loop sealing current and indicates normal current with a LED. The base unit performs bit error testing using the selected pattern. The primary or secondary channel can be tested. Another test set can be used at the far end, or a remote loopback can be manually activated to perform loop around testing.

### CSU/DSU Testing

The DDS Local Loop Interface Module can operate as a network OCU (Office Channel Unit) to test DDS CSU/DSU equipment. The module generates a loop sealing current and can also generate CSU (Channel), DSU Non Latching (Alternating) or DSU Latching loopback commands to perform looped back tests. A second test set with a V.35 or RS-232 interface module can be used to perform error rate tests straight through the CSU/DSU in a full duplex manner. The Rx level display indicates the signal strength of the CSU transmit signal.

### FRONT PANEL

The front panel uses a combination of buttons, LEDs, and displays to indicate status and perform configuration. The "switches" consist of a miniature button and a series of LEDs to indicate the switch setting. Each time the button is pressed, the next switch selection LED lights. A few seconds after a switch setting has been changed, the settings are stored in non volatile memory to retain the setup when power is turned off. The status and error LEDs have a history LED. The history LEDs indicate if the event has occurred in the past. The Reset button clears all of the history LEDs. Some combinations of switch settings are not valid. This is indicated by blinking the Setup Error LED along with the conflicting switches.

### DDS Connectors

Two 8 pin heavy duty modular RJ48S connectors, accessible from the top of the module, are used to interface to the network or CSU/DSU under test. One is labeled "To Network" and is used when the module is testing the network. The other connector is labeled "To CSU/DSU" and is used when the module is testing a CSU/DSU. The two connectors differ in the pairs used for transmit and receive. This allows testing towards the network or the CSU/DSU without the use of any crossover cables. Only one of the connectors

should be used at a time. The following table defines the pairs used for transmit and receive on each of the connectors.

| | To Network Connector | To CSU/DSU Connector |
|---|---|---|
| Transmit Data | Pins 1,2 | Pins 7,8 |
| Receive Data | Pins 7,8 | Pins 1,2 |

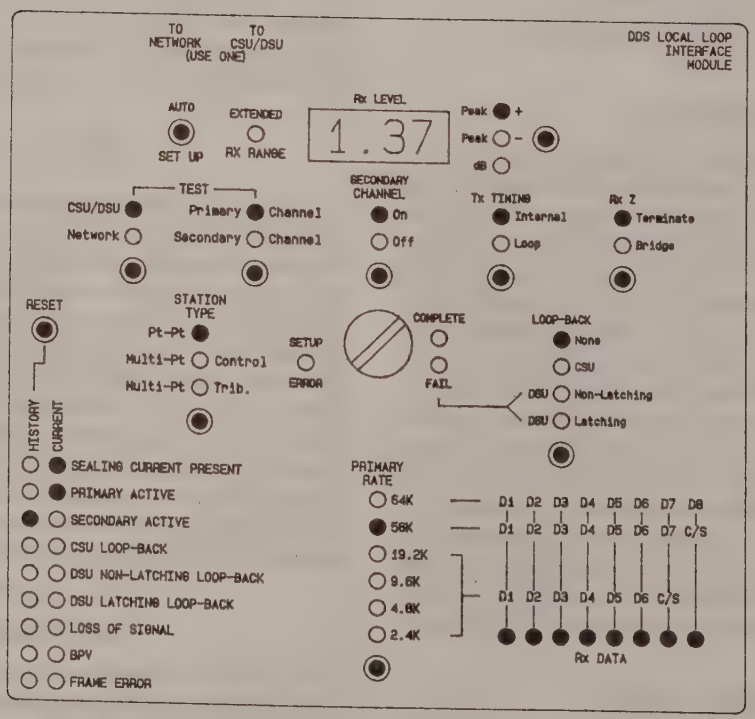
Straight (non-crossover) cables should be used when connecting to equipment for testing.

The module contains circuitry for internal protection against surges and transients.

### Auto Setup Button

Pressing this button causes the interface module to perform an auto setup based on the receive signal. The following switches are automatically set up: Test Device, Secondary Channel, Tx Timing, and Primary Rate. The Loopback is defaulted to None, Test Channel is defaulted to Primary, and Station Type is defaulted to Point-Point. Auto Setup can take over one minute to be completed. While Auto Setup is running, the level display indicates Ann where nn is the elapsed time in seconds. Some of the switch setting LEDs will change as Auto Setup runs. When Auto Setup completes, the selected level display returns and the module switch LEDs indicate the setup.

An ambiguity can occur for 64K operation, as this can look like 56K with secondary channel because both use a 72K loop rate. If this is detected, 56K with secondary channel is selected by Auto Setup.




**Full-sized line drawing of the DDS Module front panel.**

Auto Setup can be aborted at any time by pressing a button. The switch settings will be the setup that Auto Setup was trying.

### Test Device Switch

This two position switch allows selection of the device to be tested. Selections are CSU/DSU and NETWORK. The module acts as a CSU/DSU when performing network testing. The module acts as a NETWORK OCU when testing a CSU/DSU.

### Station Type Switch

This three position switch allows selection of the type of station that the module is to emulate (for TEST NETWORK mode) or test (for TEST CSU/DSU mode). Selections are PT-PT (Point to Point), MULTIPT CONTROL (Multipoint Control or Master), and MULTIPT TRIBUTARY (Multipoint Tributary or Remote. This switch controls secondary channel operation as the secondary channel encoding differs for point to point and multipoint DDS circuits. Primary channel operation is not affected. This switch is not used when the Secondary Channel is OFF. PT-PT must be selected when 64K primary rate is selected. Auto Setup always sets this switch to PT-PT.

### Secondary Channel Switch

This two position switch is used to enable or disable the secondary channel. The selections are ON and OFF. The DDS loop speed, encoding, and decoding is different for each case. When the Primary Rate is set to 64K, the secondary channel should be set to OFF as 64K does not support a secondary channel. Secondary channel testing can not be performed when the secondary channel is OFF.

### TX Timing Switch

This two position switch is used to select the timing source for transmit data. The selections are INTERNAL and LOOP. LOOP is normally selected for Network testing to allow transmit data to be clocked at the same rate as the data received from the network. INTERNAL is normally selected for CSU/DSU testing because the network is the source of timing when testing a CSU/DSU.

### RXZ Switch

This two position switch controls the impedance of the receiver. The selections are TERMINATE and BRIDGE. TERMINATE provides a normal 135 ohm impedance on the receiver. BRIDGE raises the receiver impedance to more than 1000 ohms to avoid loading a circuit that is already terminated. The TERMINATE selection is normally used for testing. BRIDGE can be used to passively monitor an operating DDS circuit. Do not connect the module transmitter when monitoring a DDS circuit to prevent corruption of the data.

### Test Channel Switch

This two position switch selects which channel to test. The selections are PRIMARY CHAN and SECONDARY CHAN. The channel not being tested is put into an idle state. A SETUP ERROR will occur if the secondary channel is OFF and the test switch is set to SECONDARY CHAN. Auto Setup always sets this switch to PRIMARY.

### Loopback Switch

This four position switch is used while testing a CSU/DSU mode to trigger CSU/DSU loop-backs. During Network testing mode, this switch allows forcing loopbacks within the interface module. The switch selections are NONE, CSU, DSU NON LATCHING, and DSU LATCHING. Loopback selections that are not valid for a setup configuration can not be made. A delay is used when making loopback switch changes, allowing the switch to be changed without initiating each loopback type switched through. When the switch is not changed for 1 second, the selected loopback is triggered. Select NONE to release the loopback. If a loopback is changed from one type to another, the first loopback is released before the second is initiated. The base unit LOOP UP/DOWN button(s) and LOOP COMPLETE LED are not used for DDS. Auto Setup always sets the loopback to NONE. The loopback selection is also defaulted to none when the module is powered up.

The base unit should be reset whenever the loopback is changed as the loopback transitions can cause pattern errors and sync losses.

### Loopback Switch Operation When Testing CSU/DSU

The CSU selection reverses the polarity of the sealing current to trigger a CSU (Channel) loopback in the CSU. The CSU loopback is supported by all DDS CSU equipment. Loopback of the attached CSU can be determined by pattern sync on the base unit. The Inject Error button can be used to confirm the loopback.

The DSU loop-backs are optionally supported by many DDS DSUs. Standard DDS supports the NON LATCHING DSU loopback, DDS with secondary channel supports both LATCHING and NON LATCHING DSU loopbacks, and 64K supports the LATCHING DSU loopback only. The DSU LOOP-BACK LEDs provide feedback on the loopback status of the DSU being tested. If the proper responses are not received from the DSU, the Fail LED will light. This can indicate that the DSU does not support the loopback selected. To retry a loopback, select NONE for a few seconds and then return the switch to the desired loopback.

When the switch position is changed, existing loopback is released. If a CSU loopback was performed, the sealing current is restored to normal polarity. If a DSU Non Latch-

ing loopback was performed, the module stops sending the alternating loopback code. If a DSU Latching loopback was performed, the loopback will be released by sending at least 35 TIP (Transition In Progress) bytes. The DSU should release the loopback after receipt of at least 31 TIP bytes. If a DSU is already in a latched loopback while the loopback switch is set to NONE, it may be released by selected DSU Latching for a few seconds then selecting NONE.

### Loopback Switch Operation When Testing Network

The module is forced into CSU or DSU loopbacks by this switch. Any network loopback commands are ignored while a loopback is forced by this switch. The loopback remains in effect until the switch is returned to NONE. While the switch is set to NONE, the module will respond to network CSU and DSU loopback commands. While a loopback is active, Rx data is looped back to the Tx. The base unit pattern generator is not used, but the base unit pattern receiver still sees the Rx data.

### Primary Rate Switch

This 6 position switch is used to select the primary channel rate. The selections are 2.4K, 4.8K, 9.6K, 19.2K, 56K, and 64K. For standard DDS, the loop rate will match the primary rate selection. For DDS with secondary channel and 64K, the loop rate is higher than the primary channel rate. Refer to the appendix for the primary channel, secondary channel, and loop rates.

### RX Level Display and Switch

The RX Level Display allows measurement of the peak positive voltage, peak negative voltage, or dB loss of the receive signal. The switch selects which measurement is to be performed. The dB loss measurement compares the peak receive signal to a nominal, no loss, level. The difference, which will approximate the loop loss, is displayed as a dB reading. The receive signal measured will be reduced by the loss in the loop when testing a network. The extended range LED indicates that the signal loss is greater than allowed in DDS specs. The level measured when testing a CSU/DSU is the transmit level of the CSU. The RxZ should be set to TERMINATE to get an accurate reading unless the receive signal is already terminated. The level meter operates on the signal pulse level and is data pattern independent. Refer to Appendix A for normal pulse amplitudes.

The Rx Level Display is also used to display error codes, auto setup elapsed time, and the firmware revision.

### Extended Range LED

This yellow LED warns when the receive signal has more than 34 dB of loss. Not all equipment will operate properly when the loop loss exceeds 34 dB. The interface module has extended range operation and can still perform testing when the loss exceeds 34 dB.

### Sealing Current Present LED

This green LED lights to indicate the presence of the loop sealing current when testing a Network. The sealing current is provided by the network to help maintain loop integrity. The current must be at least 4 mA to light the LED. The current detector is not polarity sensitive so a CSU loopback is still treated as sealing current presence.

The module provides the sealing current when testing a CSU/DSU. If sealing current is flowing through the attached CSU, the LED lights.

The red sealing current history LED lights if sealing current is ever lost. A time delay is implemented in the sealing current detector so a momentary loss of current during a polarity reversal for CSU loopbacks do not cause the history led to light.

### Primary Active LED

This green LED lights to indicate that the primary channel is active. The LED is off when the primary channel is sending an idle sequence (standard DDS) or a CMI (Control Mode Idle for DDS with secondary channel). The LED is also off when no signal is present or frame sync (for DDS with secondary channel) is not achieved. For 64K operation, the LED lights whenever frame sync is achieved as no idle state is defined.

The yellow history LED lights if the primary channel goes inactive.

### Secondary Active LED

This green LED lights to indicate that the secondary channel is active. The LED is off if the secondary channel is idle. For multipoint circuits, an idle secondary channel is defined by the occurrence of 12 mark (logical one) bits in a row. For Point to Point circuits, an idle secondary channel is defined as the occurrence of 16 mark (logical one) bits in a row. This LED does not light if the secondary channel selection switch is OFF.

The yellow history LED lights if the secondary channel becomes inactive.

### CSU Loopback LED

This yellow LED lights to indicate that a CSU (Channel) loopback is active while the module mode is testing a network. The module loops all receive data back to the transmitter within the line interface chip to allow the network to perform a loopback test. The CSU loopback is triggered by a reversal of the sealing current polarity provided by the network OCU. The module will not perform a CSU loop-

back when testing a CSU/DSU, although CSU loopbacks can be triggered in the CSU under test with the Loopback switch.

The yellow history LED lights when a CSU loopback is released. This indicates that a CSU loopback had occurred.

### DSU Non-Latching Loopback LED

This yellow LED lights to indicate that a DSU NON LATCHING (sometimes referred to as alternating) loopback is active while the module is testing a network. The loopback is triggered by reception of a loopback BPV sequence (for standard DDS) or a loopback control code (for DDS with secondary channel). While the loopback is active, the network alternates test data with loopback codes. The module loops the receive data back to the transmitter within the digital logic. The loopback terminates 4 bytes after the last loopback sequence/code. The module will not perform a DSU loopback when testing a CSU/DSU, although DSU loopbacks can be triggered in the DSU under test with the Loopback switch. Non latching loopbacks are not supported during 64K operation.

The yellow history LED lights when the DSU Non-Latching is released. This indicates that a DSU Non-Latching loopback had occurred.

### DSU Latching Loopback LED

This yellow LED lights to indicate that a DSU LATCHING LOOPBACK is active while testing a network. Latching loopbacks are triggered by a complex series of codes for DDS with secondary channel or 64K. All data is looped from the receiver to the transmitter while the loopback is active. A series of codes are needed to terminate the loopback. The module will not perform a DSU loopback when testing a CSU/DSU, although DSU loopbacks can be triggered in the DSU under test with the Loopback switch. Latching loopbacks are not supported by standard DDS.

The yellow history LED lights when the DSU Latching loopback is released. This indicates that a DSU latching loopback had occurred.

### Loss Of Signal LED

This red LED lights for a minimum of 2 seconds when no receive signal is present. A signal loss is also declared if the receive signal has a sudden increase or decrease in level that exceeds 6 dB. The base unit also displays a LOSS OF SIGNAL message. This LED may also light if the module in incorrectly configured or if the wrong DDS connector is used.

When a signal loss occurs, the module receiver attempts to re-initialize. It can take several seconds for the receiver to adapt to a new signal level. Large sudden signal strength changes do not normally occur on a DDS circuit. Changes can occur during testing when connections are made and broken.

The red history LED lights when the signal is restored. This indicates that a loss of signal had occurred.

### BPV LED

This red LED lights for a minimum of 2 seconds when an unintentional bipolar violation occurs. DDS uses an Alternate Mark Inversion (AMI) encoding scheme. Marks that do not alternate in polarity are considered to be a Bipolar Violation. Standard DDS uses some intentional BPV patterns for control purposes and zero suppression. For standard DDS, an unintentional BPV is any bipolar violation that is not part of a BPV sequence such as zero suppression or idle. For DDS with secondary channel or 64K operation, any bipolar violation is an error as BPV's are not intentionally used. The base unit also counts unintentional bipolar violations, which can be displayed in the BIPOLAR Display Mode.

For Standard DDS when testing a CSU/DSU, BPVs that are part of a zero suppression or idle pattern are not counted or indicated as an error. When testing the Network, Out of Service, Out of Frame, and Loopback patterns are also not counted.

The red history LED lights when the BPV LED goes off. This indicates that BPV(s) had occurred.

### Frame Error LED

This red LED lights for a minimum of 2 seconds when a framing pattern bit error occurs for DDS with secondary channel or 64K operation. Standard DDS does not use a framing pattern so the Frame Error LED will not light. The base unit also counts framing errors, which can be displayed in the BIPOLAR Display Mode.

Multiple framing errors will cause the module to loose frame sync and start searching for the framing pattern. If 2 out of the last 5 framing bits are in error, loss of frame sync is declared. Frame sync is displayed on a base unit LED.

The red history LED lights when the Frame Error LED goes off. This indicates that Frame Errors had occurred.

### Setup Error LED

This red LED blinks when an invalid combination of switches is set. The indication LEDs for the invalid switches also blink with the Setup Error LED to indicate which

switches are in conflict. The module is not operational while the SETUP ERROR LED is blinking. The following setup combinations are invalid:

—Test set to SECONDARY CHANNEL when the Secondary Channel is OFF.

—Secondary Channel set to ON when the Primary Rate is 64K.

—Station Type set to either MULTIPT selection when the Primary Rate is 64K.

### DSU Loopback Complete LED

This green LED lights when the proper codes have been received from the DSU to indicate that the DSU loopback has occurred when DSU NON LATCHING LOOPBACK or DSU LATCHING LOOPBACK has been selected. Note that the base unit Loop Complete LED does not operate with this module. This LED turns off when the Loopback switch is changed from a DSU selection.

### DSU Loopback Fail LED

This red LED lights when the expected codes have not been received from the DSU when DSU NON LATCHING LOOPBACK or DSU LATCHING LOOPBACK has been selected. To retry the loopback, select NONE on the Loopback switch for a few seconds and return the switch to the desired loopback. Note that not all DSUs support loopbacks. This LED goes off when the Loopback switch is changed from a DSU selection.

### RX Data LEDS

This row of 8 green LEDs display the receive data. For DDS with secondary channel and 64K, the loop byte is displayed. For standard DDS, the receive data is displayed without any particular alignment. Multiple legends are used for the LEDs because of the different loop byte structures for the different Primary Rates. The C/S (Control/Secondary Channel) LED is not used for standard DDS and will remain off. The Framing bits for DDS with secondary channel and 64K are never displayed.

### Base Unit Frame Sync LEDS

DDS with secondary channel and 64K uses a repetitive framing bit pattern to allow the receiver to align with the loop data bytes. The module receiver frame sync status is indicated by LEDs that are located on the base unit. The green FRAME SYNC LOCKED LED lights to indicate that the module receiver has achieved frame sync with the loop data for DDS with secondary channel or when operating at 64K. Once frame sync is detected, if 2 out of the last 5 framing bits are in error a loss of frame sync is declared, the FRAME SYNC LOCKED LED is turned off and a new search for the framing pattern is started. Standard DDS has no loop framing and the LED does not light. For DDS with secondary channel and 64K, the base unit displays "LOST LOCAL FRAME SYNC" while the LED is off. The base unit lights the red FRAME SYNC LOST LED if frame sync is lost.

### Base Unit RTS Switch

This base unit slide switch is used to control the active/idle state of the channel being tested. When RTS is ON, the channel under test is active and base unit data is sent. When RTS is OFF, the channel under test is put into an idle state and no base unit data is sent.

For Standard DDS, an idle BPV sequence is sent when RTS is off. For primary channel testing on DDS with secondary channel, a Control Mode Idle pattern is sent. For secondary channel testing, the secondary channel is put into a mark state when RTS is off. For 64K testing, a 7F hex idle pattern is sent while RTS is off.

To send a Data Mode Idle on standard DDS or on the primary channel for DDS with secondary channel, select the MARK pattern with NORMAL Tx DATA and RTS ON on the base unit. This will send an all ones Data Mode Idle pattern.

## GENERAL DESCRIPTION

### Power Up Self Test

At power up, the module performs an internal self test. The LED's are all lit for approximately 4 seconds. During this time, the program storage EPROM and some of the hardware are tested. If an error is detected, an error code is displayed on the level display and normal operation of the interface module is not possible. If no errors are detected, the last setup is read from the non-volatile memory and the module is set up according to the various switches.

Refer to the appendix for a list of error codes.

## SETUP

The module is set up by using the front panel buttons to make the switch selections. The LED lights next to the currently active switch selections. The proper module switch settings must be made in order to match the parameters of the DDS line and equipment under test. The SETUP ERROR LED will blink if an invalid combination of switches for a particular test are used. The LEDs for the conflicting switches also blink. The SETUP ERROR LED does not indicate if a particular switch configuration is

incorrect for the DDS link being tested. Refer to the following sections for descriptions of the valid switch settings for each of the Test Configurations. Whenever certain setup switches are changed, the module is reset. These switches are the ones that cause a major setup change and include: TEST DEVICE, STATION TYPE, SECONDARY CHANNEL, and PRIMARY RATE. When any of these are changed, the History LED's are cleared and any loopbacks are released. The base unit should also be reset any time one of these switches are changed in order to avoid the display of erroneous data.

Auto Setup can be used on an active DDS line to determine most of the setup switches. Pressing the Auto Setup button immediately starts the auto setup. Pressing any other button while auto setup is running aborts the auto setup.

Green LEDs are used for the switch selections, data display, and some of the status indications. Yellow LEDs are used to indicate loopbacks, loss of primary or secondary activity, and extended rx range operation. Red LEDs are used to indicate more serious events such as signal loss, BPV, and Frame errors. The level display indicates the selected level measurement. The level display is also used to display error codes.

Normal operation is indicated by no red or yellow LEDs lit and the frame Sync LED (on the base unit) lit for DDS with secondary channel and 64K. Note that network triggered loopbacks are a normal part of the DDS, but customer data is not passed in this case, and is indicated by yellow LEDs.

### Primary Channel Testing

There are no data restrictions for primary channel data and any base unit pattern may be used. The only exception is the latching loopback activation sequence should not be sent when operating at 64K, but this sequence is not generated by the base unit. The Test switch must be set to PRIMARY CHAN to test the primary channel. The base unit RTS switch controls the idle/active status of the transmit data. When RTS is ON, the channel is in the data mode and base unit pattern data is sent. When RTS is OFF, the module sends an idle sequence for standard DDS, and a CMI (Control Mode Idle) for DDS with secondary channel. During 64K operation the module will send a 7F hex (01111111 binary) when RTS is OFF.

For multipoint operation, the control station operates in a broadcast mode with all tributary stations receiving control station data. The data from the tributary stations is mixed by the network MJUs (Multipoint Junction Unit) for transmission to the control station. Only one tributary station should be active at a time to avoid data collisions. Normally, a polling technique is used to insure that only one tributary is active at a time. When multiple test sets are used in a multipoint environment, only one tributary should have RTS ON at a time.

### Secondary Channel Testing

For point to point DDS circuits, there are no restrictions for secondary channel data and any base unit pattern may be used. Note that the module receiver assumes the secondary channel has gone idle if 16 consecutive "1" bits occur. This may cause the SECONDARY ACTIVE LED to occasionally go off for long test patterns.

Multipoint service normally utilizes a polling technique where the control station data is broadcast to all tributary stations simultaneously. In the reverse direction, the MJUs (Multipoint Junction Unit) combine the data from the tributaries into a single data stream for delivery to the control station. Only one tributary should transmit data at one time to avoid data collisions. Note that the secondary channel operates independently from the primary channel. The tributary station that is active for secondary channel data can be different from the active primary channel tributary.

For multipoint downstream (data from the control station to all tributaries), there is no data content restriction. The module receiver assumes the secondary channel has gone idle if 16 consecutive "1" bits occur. For multipoint upstream (data from a tributary to the control station), the DDS network assumes the secondary channel is idle when 12 consecutive "1" bits occur. This is required for the MJU to detect which tributary stations have an idle secondary channel. The base unit RTS switch is used to control the channel activity. The secondary channel is forced to be idle when RTS is OFF. Base unit pattern data is enabled when RTS is ON. If test sets are connected to multiple tributaries, only one should have RTS switched on at a time. Patterns with more than 11 consecutive "1" bits should not be used for upstream testing to prevent the MJUs from detecting an idle secondary channel. The 511 and 2047 patterns do not contain more than 11 consecutive "1" bits.

When testing a CSU/DSU with a DSU loopback triggered, the secondary channel can not be directly tested. The module will default to primary channel testing when a DSU loopback is generated in the attached CSU/DSU. Secondary channel testing is restored when the loopback is released.

### Network Testing

This mode is used to test towards the network. The module emulates a CSU/DSU with pattern data generated and tested by the base unit. Another test set can be used at the other end of the DDS connection for full duplex tests. The remote CSU/DSU can also be put into a loopback mode to perform loopback tests. The module will respond to CSU and DSU loopback commands from the network. The front panel LEDs indicate loopback status. CSU or DSU loopbacks can also be forced by the Loopback switch. This overrides any network loopback commands. When the

Loopback switch is returned to NONE, the module will respond to network loopback commands.

Tx Timing will normally be set to LOOP as the network is the source of timing. INTERNAL can be used when it is desired to not use the network timing.

### CSU/DSU Testing

This mode is used to test towards the CSU/DSU. The module emulates a network OCU with pattern data generated and tested by the base unit. The module generates a sealing current with the Sealing Current Present LED indicating if the current is flowing through the CSU. The level meter indicates the transmit signal level of the CSU. This should be close to 0 dB for a normally operating CSU.

Tx Timing should be set to INTERNAL as the CSU/DSU will typically be loop timed.

CSU and DSU loopbacks can be generated to allow loopback testing in the attached CSU/DSU with only one test set. A second test set with a V.35 or RS-232 interface can be used to perform full duplex testing straight through the CSU/DSU.

### Loopbacks

DDS supports various forms of loopbacks. The network testing center uses loopbacks to determine the location of faults. All of the components in the DDS network can be looped back to sectionalize a fault. The loopbacks of interest to the DDS interface module are the CSU and DSU loopbacks. The module can generate or respond to both types of loopbacks dependent on the setup. All CSU/DSU equipment should support the CSU loopback. The DSU loopbacks are optional and may be supported.

The CSU loopback (channel loopback) is done as close to the network interface as possible. The receive data is filtered and equalized then sent to the transmitter. Data content and any bipolar violations are not changed. This minimizes penetration into the CSU/DSU to allow the network to perform a test of the loop between the network OCU and customer CSU. This allows isolation of trouble to the either the network or customer equipment. A CSU loopback is triggered by reversing the polarity of the loop simplex sealing current.

The DSU loopbacks are used to loop data back close to the EIA/CCITT interface (such as RS-232 or V.35) to test as much of the CSU/DSU as possible. This is designed to provide maximum penetration into the customer equipment to isolate trouble to the CSU/DSU or connected terminal equipment. Two types of DSU loopbacks can be performed, latching and non-latching (also known as alternating). DSU loopbacks are triggered by special code words (non-latching) or a complex series of codes (latching). Standard DDS only supports the non-latching DSU loopback. DDS with secondary channel supports both the latching and non-latching DSU loopbacks. 64K supports only the latching DSU loopback.

### Loopbacks when Testing CSU/DSU

The DDS interface module generates loopback commands when testing a CSU/DSU. The Loopback switch is used to trigger the desired loopback in the CSU/DSU. The module will not respond to any loopback commands.

If Tx Timing is set to LOOP, internal timing will be used when performing loopbacks. This is to ensure a clock source while the CSU/DSU is using loop timing during the loopback. When the loopback is released, the module will restore loop timing.

When the Loopback switch is set to CSU, the polarity of the generated simplex sealing current is reversed. This should trigger the attached CSU to loopback. This can be verified by the loopback indications on the CSU or by using the INJECT ERROR button on the base unit. If the CSU is looped back, an error should be counted. There is no indication on the module of a completed CSU loopback.

A DSU Non-Latching loopback can be generated (except for 64K testing) by setting the Loopback switch to DSU NON-LATCHING. The module will send 10 non-latching loopback codes then start alternating base unit pattern data with loopback codes. If an alternating pattern is received within 2 seconds, the COMPLETE LED is lit and pattern testing can be performed by the base unit. If no alternating pattern is received within 2 seconds, the FAIL led is lit and the alternating loopback pattern is stopped. The loopback codes received from the looped back DSU are not passed to the base unit allowing testing on the alternate data bytes. The effective bit rate during testing is half the normal rate. The loopback is released by stopping the alternating loopback/data pattern.

A DSU Latching loopback can be generated (except for Standard DDS) by setting the Loopback switch to DSU LATCHING. The module will send the Latching series of codes as follows:

1. 50 TIP (Transition In Progress) codes are sent.

2. 45 LSC (Loopback Select) codes with the DSU device code are sent.

3. 110 LBE (Loop Back Enable) codes are sent.

4. FEV (Far End Voice) codes are sent for up to 2 seconds. If the receiver detects 50 FEV codes returned from the DSU, the PASS LED is lit and base unit data is sent. If 50 FEV codes are not detected within 2 seconds, the FAIL LED is lit and base unit data is sent.

The DSU Latching loopback is released by sending 50 TIP codes when the Loopback switch is changed from DSU LATCHING. If the DSU is in a Latched DSU Loopback while the switch is set to NONE, it can be released by selecting DSU LATCHED for several seconds then returning the switch to NONE.

### Loopbacks when Testing Network

While testing the network, the DDS interface module will respond to loopback commands generated by the network. The loopback switch can be also used to force CSU or DSU loopbacks if desired. The DSU LOOPBACK COMPLETE and FAIL LEDs do not operate when testing the network. The DSU NON-LATCHING LOOPBACK, DSU LATCHING LOOPBACK, and CSU LOOPBACK LEDs indicate the status of any network generated loopbacks. The History LEDs indicate if any loopbacks had been performed in the past. While a loopback is active, base unit data is not sent. The base unit pattern receiver will still see the received data. The received data can contain various patterns and codes that are generated by the Network testing center.

If the Tx Timing is set to INTERNAL, loop timing will be used for the duration of the loopback. This is because the transmit data must be loop timed during a loopback. When the loopback is released, internal timing will resume.

The module will perform a CSU loopback if the polarity of the simplex sealing current is reversed from normal. The loopback will remain until the polarity returns to normal. If the sealing current is removed, the loopback will also be dropped. During a CSU loopback, all received data, including any errors, is looped back to the transmitter.

The module will perform a DSU Non-latching loopback (except for 64K) if at least 4 consecutive loopback codes are received. The loopback will continue until 4 consecutive non loopback codes are received. During the loopback test, the network will alternate test and loopback codes to maintain the loopback. For DDS with secondary channel, the module will map the loopback code to return a byte of N010000F1 for 56K and 010000F1 for subrates. For standard DDS the module will correct the BPV in the loopback code word when returned.

The module will perform a DSU Latching loopback (except for standard DDS) if the proper sequence of codes is received. The following sequence must be received in the order listed:

1. A minimum of 35 TIP codes.
2. A minimum of 35 LSC codes with DSU as the selected device.
3. A minimum of 100 LBE codes.
4. A minimum of 32 FEV codes.

After this sequence is received, all received data is looped back. While the loopback is active, any sequence of more than 30 LBE codes are mapped to produce the byte S001001F1. This mapping is terminated upon the receipt of 3 non-LBE bytes. The mapping resumes if 30 LBE codes are received. The latching loopback is released after receiving 31 TIP codes.

## SPECIFICATIONS

The DDS Local Loop Interface Module meets the applicable sections of AT&T Pub 62310, Bellcore Pub 62310, Bellcore TR-NPL-000157, and Pacific Bell/Nevada Bell PUB L-780077-PB/NB.

Power +5 Vdc, 320 mA Max.
+12 Vdc, 93 mA Max.
-12 Vdc, 43 mA Max.
(Provided by base unit via mating 37 Pin "D" Connector)
DDS Connectors: Two 8 position USOC RJ48S, connected as follows:

| | To Network Connector | To CSU/DSU Connector |
|---|---|---|
| Transmit Data | Pins 1,2 | Pins 7,8 |
| Receive Data | Pins 7,8 | Pins 1,2 |

DDS Output 135 ohm impedance
Pulse amplitude into 135 ohm resistive load
At 9.6K primary rate: 0.72V to 0.88V

DDS Input Switchable 135 ohm or >1K ohm impedance
Automatic equalization for lines with losses of up to 40 dB for loop rates of 56K and 72K
Extended range indication when loss exceeds 34 dB

Internal Clock Accuracy 50 ppm

Level Meter
Range 0.0V to 3.0V peak
-50 dB to +9 dB @ 9600
-50 dB to +6 dB at all other primary rates
Resolution 0.01V, 1 dB
Accuracy +/-5% of actual peak voltage
+/-1 dB for signals +6 dB to -29 dB

Extended Range Threshold 34dB +/-1 dB loss with respect to a nominal level

| | |
|---|---|
| Sealing (Simplex) Current detection threshold: | 3.9 to 4.1 mA, either polarity |
| Sealing (Simplex) Current when testing CSUDSU | 25V maximum open circuit voltage<br>20 mA maximum short circuit current |
| Non-volatile Setup Memory Lifetime: | More than 1 million write cycles |
| Enclosure | Plastic Molded |
| PC Boards | Two |
| Dimensions | 5.95"L x 5.60"W x 1.40"D |
| Weight | Less than 1 lb. |
| Temperature | Operating: 0° to 50°C<br>(+21F to +122F)<br><br>Storage: -20° to +70° C<br>(-4F to +150F) |
| Humidity | 90% maximum (non-condensing) |

## APPENDIX A
## PRIMARY RATE, SECONDARY RATE, LOOP RATE, AND PULSE LEVEL TABLE

| Primary Rate | Secondary Rate | Loop Rate | Pulse Level |
|---|---|---|---|
| 2.4K | N/A | 2.4K | 1.4V |
| 2.4K | 133.3 | 3.2K | 1.4V |
| 4.8K | N/A | 4.8K | 1.4V |
| 4.8K | 266.7 | 6.4K | 1.4V |
| 9.6K | N/A | 9.6K | 0.79V |
| 9.6K | 533.3 | 12.8K | 0.79V |
| 19.2K | N/A | 19.2K | 1.4V |
| 19.2K | 1067 | 25.6K | 1.4V |
| 56K | N/A | 56K | 1.4V |
| 56K | 2667 | 72K | 1.4V |
| 64K | N/A | 72K | 1.4V |

Notes:

—The secondary rate is based on 1 out of 3 C/S bits being used for secondary channel data. The interface module does not support any other secondary encoding methods.

—The Pulse Level is for a 135 Ohm resistive terminated signal with no cable loss.

—The Loop Rate is higher than the primary channel rate to allow for the secondary channel, control bits, and framing pattern. 64K also uses a loop framing pattern and has a higher loop speed.

## APPENDIX B
## ERROR CODE DISPLAYS

The level display is also used to display error codes, auto setup elapsed time, and the Firmware Revision. Self test error codes have the format E0n where n is the test that failed. Run Time error codes have the format E1n where n is the detected failure. The auto setup display format is Ann where nn is the elapsed time that the setup has been running in seconds.

### Self Test Error Codes

The following codes can be displayed at power up after self test runs:

| Code | Test Failure |
|---|---|
| E01 | EPROM Checksum Error |
| E02 | Button Group 1 Error |
| E03 | Button Group 2 Error |
| E04 | Unable to load FPGA |
| E05 | Setup EEPROM contents missing or multiple |

The Button errors indicate that Self Test detected a pressed button. If a button is pressed while self test runs, a false button error can occur. The FPGA is a Field Programmable Gate Array that has to be loaded by the CPU in the module. The EEPROM is used to retain switch settings while power is off. It is scanned by self test for missing or multiple setups. If an error is detected, it is erased and loaded with a default setup.

### Run Time Error Codes

The following error codes can occur at any time if failures are detected while the module is running:

| Code | Test Failure |
|---|---|
| E11 | Unable to load FPGA |
| E12 | Auto Setup unable to determine setup |
| E13 | Invalid setup read from EEPROM |
| E14 | Tx Clock not active |
| E15 | Rx Clock not active |
| E16 | Watchdog Timeout occurred |

If an invalid setup is read from the EEPROM, a default setup is used and is also written to the EEPROM. The Tx and Rx clocks are internal to the module and are required for operation. They should always be present even if no Rx signal is present. The FPGA is used to contain most of the module logic. It is loaded with different logic designs depending on the setup switches. A watchdog timer runs to detect if the CPU in the module gets hung up. Normal operation keeps this timer set. If it times out, the CPU may have crashed or hung up.

### Auto Setup Elapsed Time

While Auto Setup is running, the level display indicates Ann where nn is the elapsed time in seconds. This is to indicate that auto setup is still in progress. Auto Setup can take over one minute.

### Firmware Revision

The revision of the internal firmware is displayed after the powerup lamptest. It is displayed as rN.N where N.N is the firmware revision such as 1.0. Note this revision when contacting IDS Technical Support with any questions.

## APPENDIX C
## DDS STRESS PATTERNS

The Model 77 base unit provides a wide variety of patterns to perform error rate testing. Various stress patterns are used during DDS network testing in addition to pseudo random patterns. Since the Model 77 was designed as a general purpose high speed test set, some of these specific patterns for DDS stress testing can not be generated. The 511 and 2047 patterns are also commonly used for network testing can be generated by the Model 77. The DDS3 and DDS4 stress patterns can be generated by the Model 77. To test using the DDS3 stress pattern, setup the USER1 pattern to be 8 bits long and enter the pattern 01001100 into USER1. Select USER1 as the PATTERN. The DDS4 stress pattern testing can be done by selecting 1 IN 8 as the PATTERN on the Model 77.

The longer pseudo random patterns, such as the 32K, 1M ($2^{20}$-1) and 8M ($2^{23}$-1) better simulate actual data and also can be used for effective error rate testing. These longer patterns contain a much larger variety of data patterns that the 511 and 2047 patterns.

The MARK pattern can be used to simulate a data mode idle condition and stress the equipment with a very high one's density. To perform testing with zero's, select the MARK pattern with Tx DATA set to INVERT. This will stress the equipment with a very low one's density and also check the zero suppression for standard DDS.

## APPENDIX D
## APPLICATIONS

The Model 77 with the DDS Local Loop Interface Module performs testing on the DDS four wire customer loop. Tests can be performed in one of two directions, toward the network or towards the customer CSU/DSU.

Testing toward the network is "typical" DDS local loop testing and allows testing of the local loop itself, the OCU and other network equipment in the serving office and network. If two test sets are used with one at each end of a point to point DDS link, complete full duplex testing can be done. This performs a good test of the overall network from customer site to customer site. The DDS Interface Module also will respond to network generated loopback commands to allow isolation testing to be performed. The level meter displays the strength of the received signal and indicates if the level is within DDS specifications. LOOP Tx Timing is normally used when testing the network.

Testing toward the CSU/DSU allows testing operation of the CSU/DSU in a stand alone manner. This can be used to confirm operation before installation or to isolate problems. The module generates a sealing current and uses internal Tx timing so the CSU/DSU think they are connected to a network OCU. The module can generate loopback commands to perform loop around testing of the CSU or DSU. A second test set with a V.35 or RS-232 interface can be used to perform full duplex testing through the CSU/DSU to provide a complete operational test. The level meter displays the strength of the CSU transmit signal. It should be close to 0 dB. INTERNAL Tx Timing is used when testing a CSU/DSU as the CSU/DSU is normally loop timed.

If the module receiver is tapped across a DDS line in bridge mode, some performance monitoring can be accomplished. The CSU output can be monitored by connecting the module receiver to the Tx pair. The network can be monitored by connecting the module receiver to the Rx pair. The Loss of Signal, Frame Error, BPV, Primary Active, and Secondary Active LEDs all will function. The data LEDs will display the monitored data. The base unit can count BPV and Frame errors. Auto Setup can be used to determine what speed and format the line is using. The level meter displays the level of the Rx signal. The Sealing Current Present LED will not light because the network sealing current will not flow through the module with this connection.

## APPENDIX E
## ACCESSORIES AND OPTIONS

The following accessories are provided with the DDS Local Loop Interface Module:

1) 6' RJ48 to RJ48 Cable
2) Manual

The following options are available from IDS.

1) 6' RJ48 to Alligator Clip cable

This option allows connection to DDS lines or equipment that does not use an RJ48S jack

2) Loopback Plug

This option allows a quick confirmation of the DDS Interface Module operation. When plugged into the To Network or To CSU/DSU jack, the module receiver is connected to the transmitter. A BERT test can be performed by the Model 77 to confirm module operation.

## WARRANTY AND REPAIR

### WARRANTY

The IDS Bit Error Rate Testers and Interface Modules are warranted for three (3) years against defects in material, workmanship, and component failure. Units repaired by IDS are warranted for 90 days following the repair service.

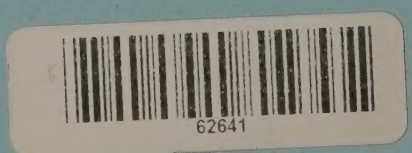
This warranty does not apply if the equipment has been damaged by accident, neglect, misuse, or causes other than ordinary use, or as a result of service or modification other than performed or authorized by IDS.

### REPAIR

Should your unit require repairs not covered by the original warranty, IDS will perform the repair at an hourly charge plus parts. Normal turn-around time is two weeks.

Prior to shipping your unit, contact IDS at 1-800-IDS-DATA for a Return Authorization (RA) number. All transportation charges are the responsibility of the purchaser. Please include a purchase order that clearly states where the unit is to be returned to.

Units for repair should be sent to International Data Sciences, Inc., 501 Jefferson Blvd., Warwick, RI 02886-1317, Attention: Repair Department, Ref: RA#_____.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